

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J92 MLB NEWARK - DVT

11/21/2014

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

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ALIASES RESOLVED

PRODUCT SAFETY REQUIREMENTS:
PCB, UL RECOGNIZED, MIN. 130-C TEMP. RATING AND V-0 FLAME RATING PER UL 796 & UL 94.
PCB TO BE SILK-SCREENED WITH UL/CUL RECOGNITION MARK, MANUFACTURER'S UL FILE
NUMBER, UL PCB MATERIAL DESIGNATION, 130-C TEMP. RATING AND V-0 FLAME RATING.

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00107	1	SCHEM,MLB-NEWARK,J92	SCH	CRITICAL	
820-00045	1	PCBF,MLB-NEWARK,J92	PCB	CRITICAL	

DRAWING TITLE		DRAWING NUMBER		SIZE
<PART_DESCRIPTION>		<SCH_NUM>	D	
 Apple Inc.		REVISION		
		<E4LABEL>		
NOTICE OF PROPRIETARY PROPERTY:		BRANCH		
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D	Top level BOM Variants																																																																																																																																																																																																																																																																														
	<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>639-6568</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6569</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6570</td><td>PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6571</td><td>PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6572</td><td>PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6573</td><td>PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6574</td><td>PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6575</td><td>PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6576</td><td>PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td rowspan="10">C</td><td>639-6577</td><td>PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6578</td><td>PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6579</td><td>PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr><tr><td>639-6580</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6581</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6582</td><td>PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6583</td><td>PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6584</td><td>PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6585</td><td>PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6586</td><td>PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td rowspan="10">B</td><td>639-6587</td><td>PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6588</td><td>PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6589</td><td>PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6590</td><td>PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6591</td><td>PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP</td></tr><tr><td>639-6592</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6593</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6594</td><td>PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6595</td><td>PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6596</td><td>PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td rowspan="10">A</td><td>639-6597</td><td>PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6598</td><td>PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6599</td><td>PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6600</td><td>PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6601</td><td>PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6602</td><td>PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6603</td><td>PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92</td><td>ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP</td></tr><tr><td>639-6604</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI IND,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP</td></tr><tr><td>639-6605</td><td>PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI IND,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP</td></tr><tr><td>639-6606</td><td>PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI IND,J92</td><td>ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP</td></tr><tr><td colspan="9"><table><tr><td colspan="2">Partial & development BOMs</td></tr><tr><td>BOM NUMBER</td><td>BOM NAME</td><td>BOM OPTIONS</td></tr><tr><td>685-00014</td><td>CMN PTS,PCBA,MLB-NEWARK,J92</td><td>MLB_COMMON</td></tr><tr><td>685-00003</td><td>POP,MLB,S1X-A2,ELP-4GBIT,X261</td><td>S1X:A2,S1X_DRAM:ELPIDA</td></tr><tr><td>685-00004</td><td>POP,MLB,S1X-A2,HYN-4GBIT,X261</td><td>S1X:A2,S1X_DRAM:HYNIX</td></tr><tr><td>939-00043</td><td>PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261</td><td>ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr></table></td></tr><tr><td colspan="9"><table><tr><td colspan="6">Common BOM</td></tr><tr><td>PART NUMBER</td><td>QTY</td><td>DESCRIPTION</td><td>REFERENCE DES</td><td>CRITICAL</td><td>BOM OPTION</td></tr><tr><td>685-00014</td><td>1</td><td>CMN PTS,PCBA,MLB-NEWARK,J92</td><td>CMNPPTS</td><td>CRITICAL</td><td>CMN</td></tr></table></td></tr><tr><td colspan="9"><table><tr><td colspan="6">Programmable Parts</td></tr><tr><td>PART NUMBER</td><td>QTY</td><td>DESCRIPTION</td><td>REFERENCE DES</td><td>CRITICAL</td><td>BOM OPTION</td></tr><tr><td>341S00196</td><td>1</td><td>BT ROM (VXX) DVT,2MBIT,X261</td><td>U3570</td><td>CRITICAL</td><td>BT:PROG</td></tr><tr><td>341S00197</td><td>1</td><td>WIFI ROM (PXXXX) DVT,WW1,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:FCC</td></tr><tr><td>341S00198</td><td>1</td><td>WIFI ROM (PXXXX) DVT,WW2,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:ETSI</td></tr><tr><td>341S00199</td><td>1</td><td>WIFI ROM (PXXXX) DVT,WW3,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:APAC</td></tr><tr><td>341S00200</td><td>1</td><td>WIFI ROM (PXXXX) DVT,IND,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:IND</td></tr></table></td></tr><tr><td colspan="9"><table><tr><td colspan="6">BOM Groups</td></tr><tr><td>BOM GROUP</td><td colspan="5">BOM OPTIONS</td></tr><tr><td>MLB_PROGPARTS</td><td colspan="5">BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG</td></tr></table></td></tr><tr><td></td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td></tr></table>								BOM NUMBER	BOM NAME	BOM OPTIONS	639-6568	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6569	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6570	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6571	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6572	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6573	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6574	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6575	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6576	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	C	639-6577	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6578	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6579	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	639-6580	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6581	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6582	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6583	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6584	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6585	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6586	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	B	639-6587	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6588	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6589	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6590	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6591	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP	639-6592	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6593	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6594	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6595	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6596	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	A	639-6597	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6598	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6599	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6600	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6601	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6602	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6603	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP	639-6604	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP	639-6605	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP	639-6606	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP	<table><tr><td colspan="2">Partial & development BOMs</td></tr><tr><td>BOM NUMBER</td><td>BOM NAME</td><td>BOM OPTIONS</td></tr><tr><td>685-00014</td><td>CMN PTS,PCBA,MLB-NEWARK,J92</td><td>MLB_COMMON</td></tr><tr><td>685-00003</td><td>POP,MLB,S1X-A2,ELP-4GBIT,X261</td><td>S1X:A2,S1X_DRAM:ELPIDA</td></tr><tr><td>685-00004</td><td>POP,MLB,S1X-A2,HYN-4GBIT,X261</td><td>S1X:A2,S1X_DRAM:HYNIX</td></tr><tr><td>939-00043</td><td>PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261</td><td>ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr></table>									Partial & development BOMs		BOM NUMBER	BOM NAME	BOM OPTIONS	685-00014	CMN PTS,PCBA,MLB-NEWARK,J92	MLB_COMMON	685-00003	POP,MLB,S1X-A2,ELP-4GBIT,X261	S1X:A2,S1X_DRAM:ELPIDA	685-00004	POP,MLB,S1X-A2,HYN-4GBIT,X261	S1X:A2,S1X_DRAM:HYNIX	939-00043	PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261	ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP	<table><tr><td colspan="6">Common BOM</td></tr><tr><td>PART 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DVT,WW3,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:APAC</td></tr><tr><td>341S00200</td><td>1</td><td>WIFI ROM (PXXXX) DVT,IND,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:IND</td></tr></table>									Programmable Parts						PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	341S00196	1	BT ROM (VXX) DVT,2MBIT,X261	U3570	CRITICAL	BT:PROG	341S00197	1	WIFI ROM (PXXXX) DVT,WW1,X261	U3580	CRITICAL	WIFI:FCC	341S00198	1	WIFI ROM (PXXXX) DVT,WW2,X261	U3580	CRITICAL	WIFI:ETSI	341S00199	1	WIFI ROM (PXXXX) DVT,WW3,X261	U3580	CRITICAL	WIFI:APAC	341S00200	1	WIFI ROM (PXXXX) DVT,IND,X261	U3580	CRITICAL	WIFI:IND	<table><tr><td colspan="6">BOM Groups</td></tr><tr><td>BOM GROUP</td><td colspan="5">BOM OPTIONS</td></tr><tr><td>MLB_PROGPARTS</td><td colspan="5">BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG</td></tr></table>									BOM Groups						BOM GROUP	BOM OPTIONS					MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG						8	7	6	5	4	3	2	1
	BOM NUMBER	BOM NAME	BOM OPTIONS																																																																																																																																																																																																																																																																												
	639-6568	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6569	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6570	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6571	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6572	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6573	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6574	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
639-6575	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																													
639-6576	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																													
C	639-6577	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6578	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6579	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI FCC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6580	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6581	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6582	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6583	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6584	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6585	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6586	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
B	639-6587	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6588	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6589	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6590	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6591	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI ETSI,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:ETSI,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6592	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6593	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6594	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6595	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6596	PCBA,MLB,1.2GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
A	639-6597	PCBA,MLB,1.2GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6598	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6599	PCBA,MLB,1.2GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.2GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6600	PCBA,MLB,1.3GHZ,EL 8GB,SAND 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6601	PCBA,MLB,1.3GHZ,EL 8GB,SAND 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6602	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 256G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6603	PCBA,MLB,1.3GHZ,EL 8GB,TOSH 512G,WIFI APAC,J92	ALTERNATE,CMN,CPU:1.3GHZ,DRAM:ELP_8GB,NAND:TOSH_512GB_1Y_128GBIT,WIFI:APAC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6604	PCBA,MLB,1.1GHZ,EL 8GB,SAND 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6605	PCBA,MLB,1.1GHZ,EL 8GB,SAND 512G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:SAND_512GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
	639-6606	PCBA,MLB,1.1GHZ,EL 8GB,TOSH 256G,WIFI IND,J92	ALTERNATE,CMN,CPU:1.1GHZ,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:IND,SSDRAM:A1_ELP																																																																																																																																																																																																																																																																												
<table><tr><td colspan="2">Partial & development BOMs</td></tr><tr><td>BOM NUMBER</td><td>BOM NAME</td><td>BOM OPTIONS</td></tr><tr><td>685-00014</td><td>CMN PTS,PCBA,MLB-NEWARK,J92</td><td>MLB_COMMON</td></tr><tr><td>685-00003</td><td>POP,MLB,S1X-A2,ELP-4GBIT,X261</td><td>S1X:A2,S1X_DRAM:ELPIDA</td></tr><tr><td>685-00004</td><td>POP,MLB,S1X-A2,HYN-4GBIT,X261</td><td>S1X:A2,S1X_DRAM:HYNIX</td></tr><tr><td>939-00043</td><td>PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261</td><td>ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP</td></tr></table>									Partial & development BOMs		BOM NUMBER	BOM NAME	BOM OPTIONS	685-00014	CMN PTS,PCBA,MLB-NEWARK,J92	MLB_COMMON	685-00003	POP,MLB,S1X-A2,ELP-4GBIT,X261	S1X:A2,S1X_DRAM:ELPIDA	685-00004	POP,MLB,S1X-A2,HYN-4GBIT,X261	S1X:A2,S1X_DRAM:HYNIX	939-00043	PCBA,MLB,NO CPU,EL 8GB,TOSH 256G,WIFI FCC,X261	ALTERNATE,CMN,DRAM:ELP_8GB,NAND:TOSH_256GB_1Y_128GBIT,WIFI:FCC,SSDRAM:A1_ELP																																																																																																																																																																																																																																																						
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<table><tr><td colspan="6">Common BOM</td></tr><tr><td>PART NUMBER</td><td>QTY</td><td>DESCRIPTION</td><td>REFERENCE DES</td><td>CRITICAL</td><td>BOM OPTION</td></tr><tr><td>685-00014</td><td>1</td><td>CMN PTS,PCBA,MLB-NEWARK,J92</td><td>CMNPPTS</td><td>CRITICAL</td><td>CMN</td></tr></table>									Common BOM						PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	685-00014	1	CMN PTS,PCBA,MLB-NEWARK,J92	CMNPPTS	CRITICAL	CMN																																																																																																																																																																																																																																																					
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<table><tr><td colspan="6">Programmable Parts</td></tr><tr><td>PART NUMBER</td><td>QTY</td><td>DESCRIPTION</td><td>REFERENCE DES</td><td>CRITICAL</td><td>BOM OPTION</td></tr><tr><td>341S00196</td><td>1</td><td>BT ROM (VXX) DVT,2MBIT,X261</td><td>U3570</td><td>CRITICAL</td><td>BT:PROG</td></tr><tr><td>341S00197</td><td>1</td><td>WIFI ROM (PXXXX) DVT,WW1,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:FCC</td></tr><tr><td>341S00198</td><td>1</td><td>WIFI ROM (PXXXX) DVT,WW2,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:ETSI</td></tr><tr><td>341S00199</td><td>1</td><td>WIFI ROM (PXXXX) DVT,WW3,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:APAC</td></tr><tr><td>341S00200</td><td>1</td><td>WIFI ROM (PXXXX) DVT,IND,X261</td><td>U3580</td><td>CRITICAL</td><td>WIFI:IND</td></tr></table>									Programmable Parts						PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	341S00196	1	BT ROM (VXX) DVT,2MBIT,X261	U3570	CRITICAL	BT:PROG	341S00197	1	WIFI ROM (PXXXX) DVT,WW1,X261	U3580	CRITICAL	WIFI:FCC	341S00198	1	WIFI ROM (PXXXX) DVT,WW2,X261	U3580	CRITICAL	WIFI:ETSI	341S00199	1	WIFI ROM (PXXXX) DVT,WW3,X261	U3580	CRITICAL	WIFI:APAC	341S00200	1	WIFI ROM (PXXXX) DVT,IND,X261	U3580	CRITICAL	WIFI:IND																																																																																																																																																																																																																													
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<table><tr><td colspan="6">BOM Groups</td></tr><tr><td>BOM GROUP</td><td colspan="5">BOM OPTIONS</td></tr><tr><td>MLB_PROGPARTS</td><td colspan="5">BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG</td></tr></table>									BOM Groups						BOM GROUP	BOM OPTIONS					MLB_PROGPARTS	BOOTROM:PROG,BT:PROG,SMC:PROG,SSDROM:PROG,HPM:PROG																																																																																																																																																																																																																																																									
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SYNC DATE=10/24/2012

PAGE TITLE

J92 BOM Variants

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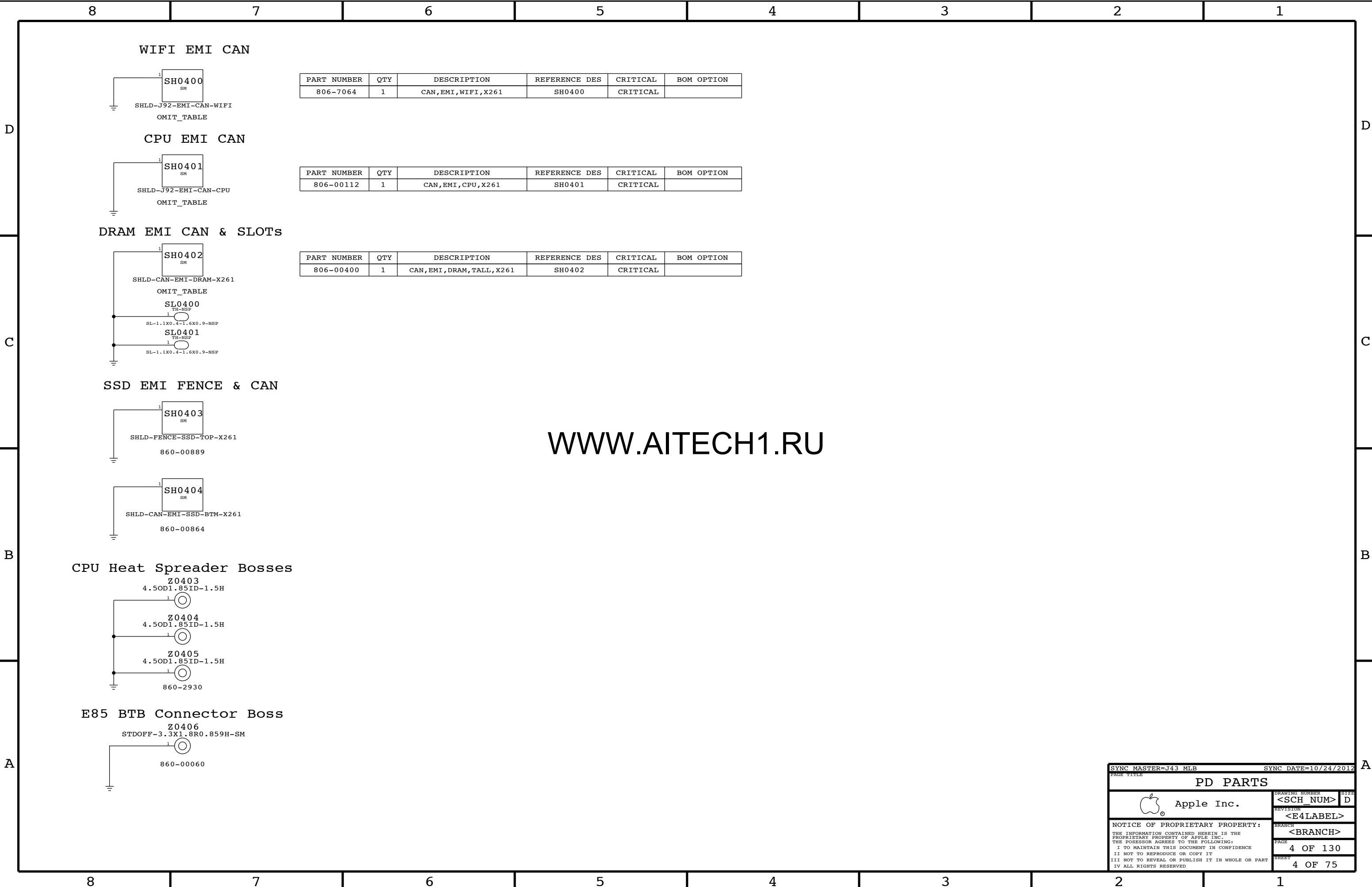
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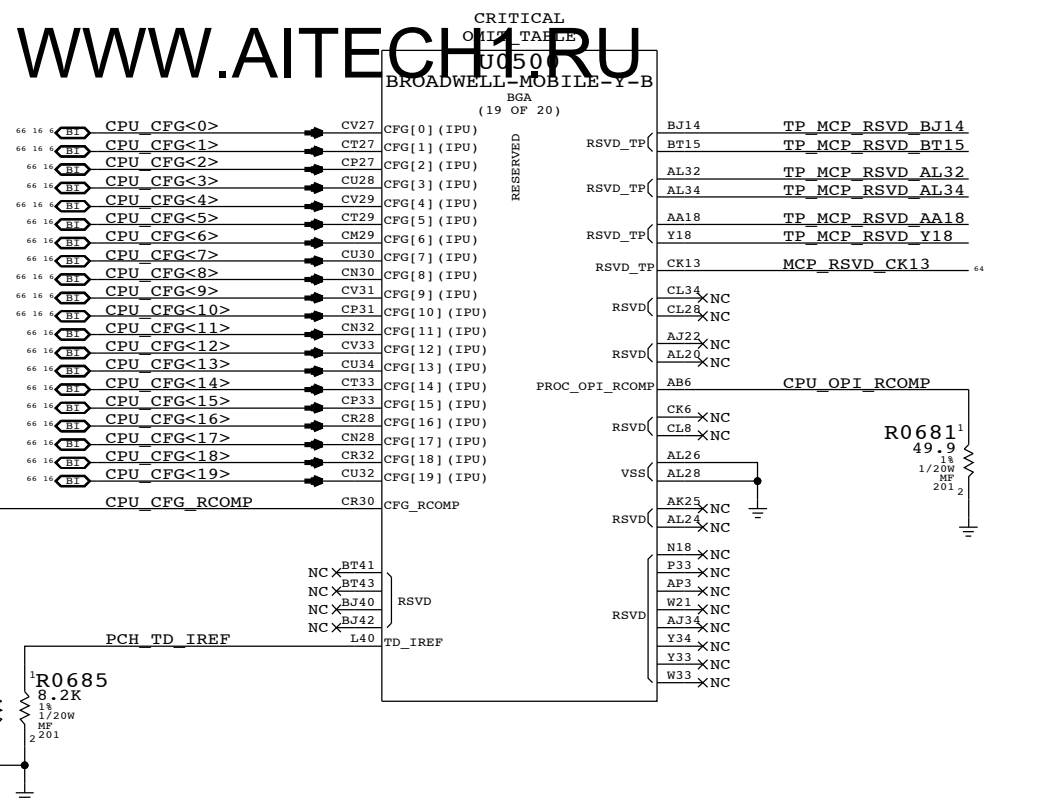
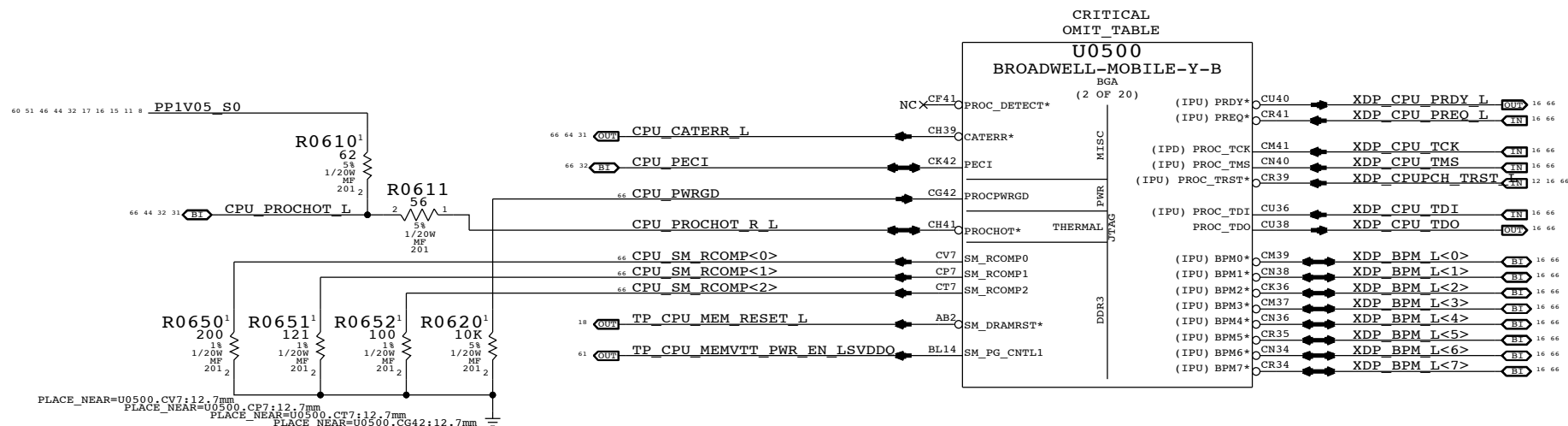
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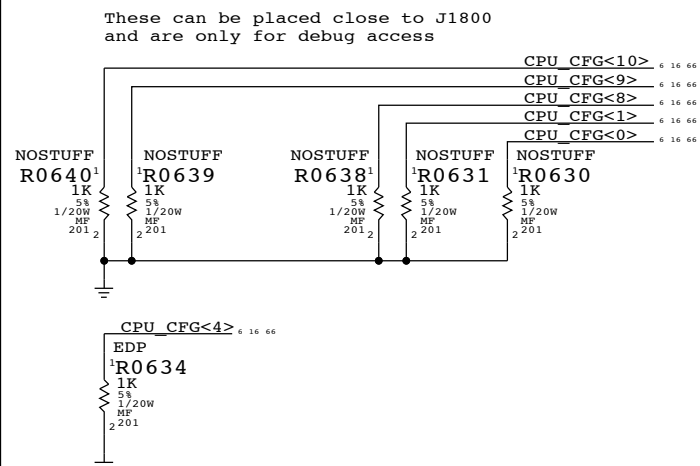
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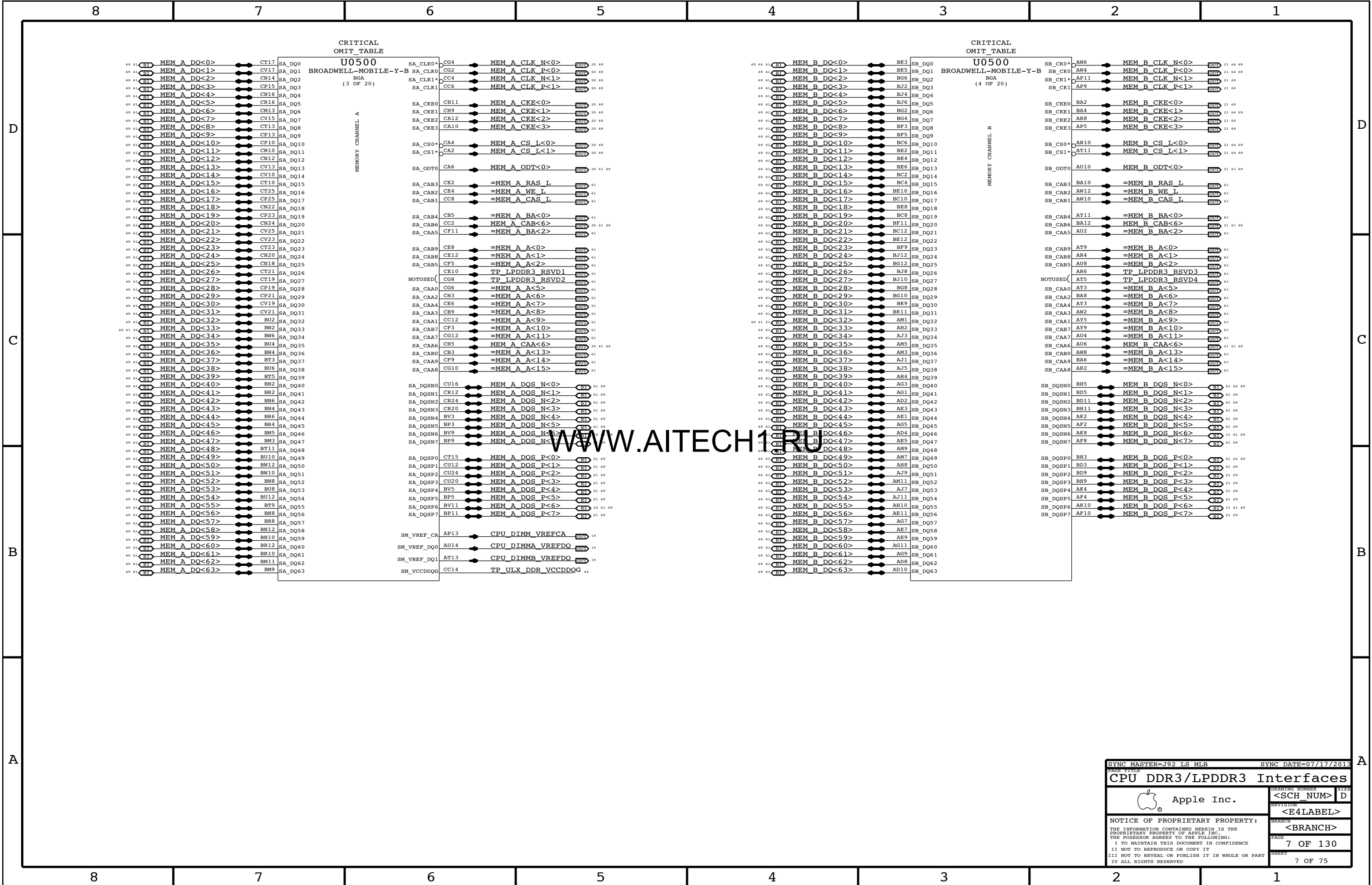
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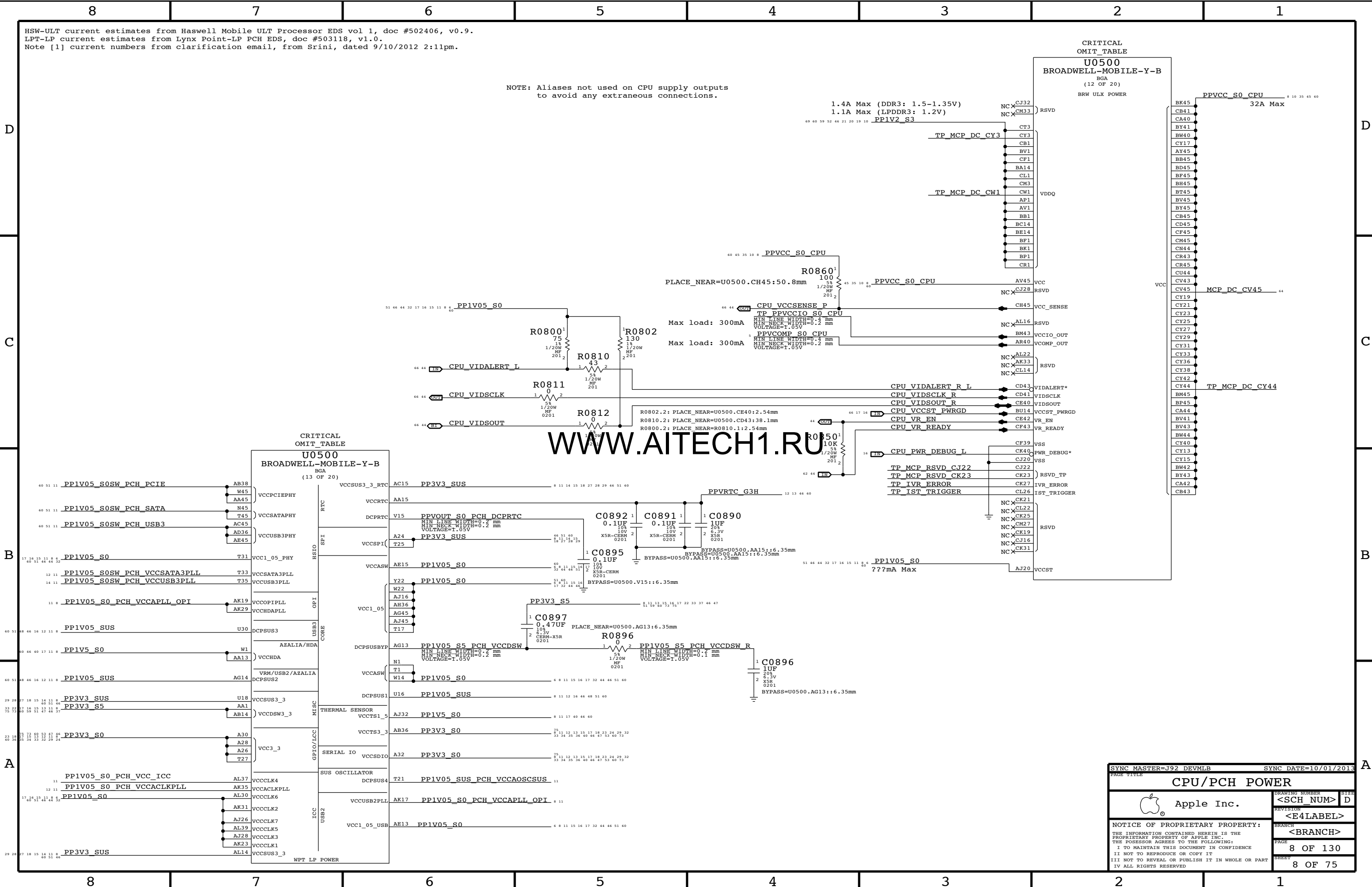



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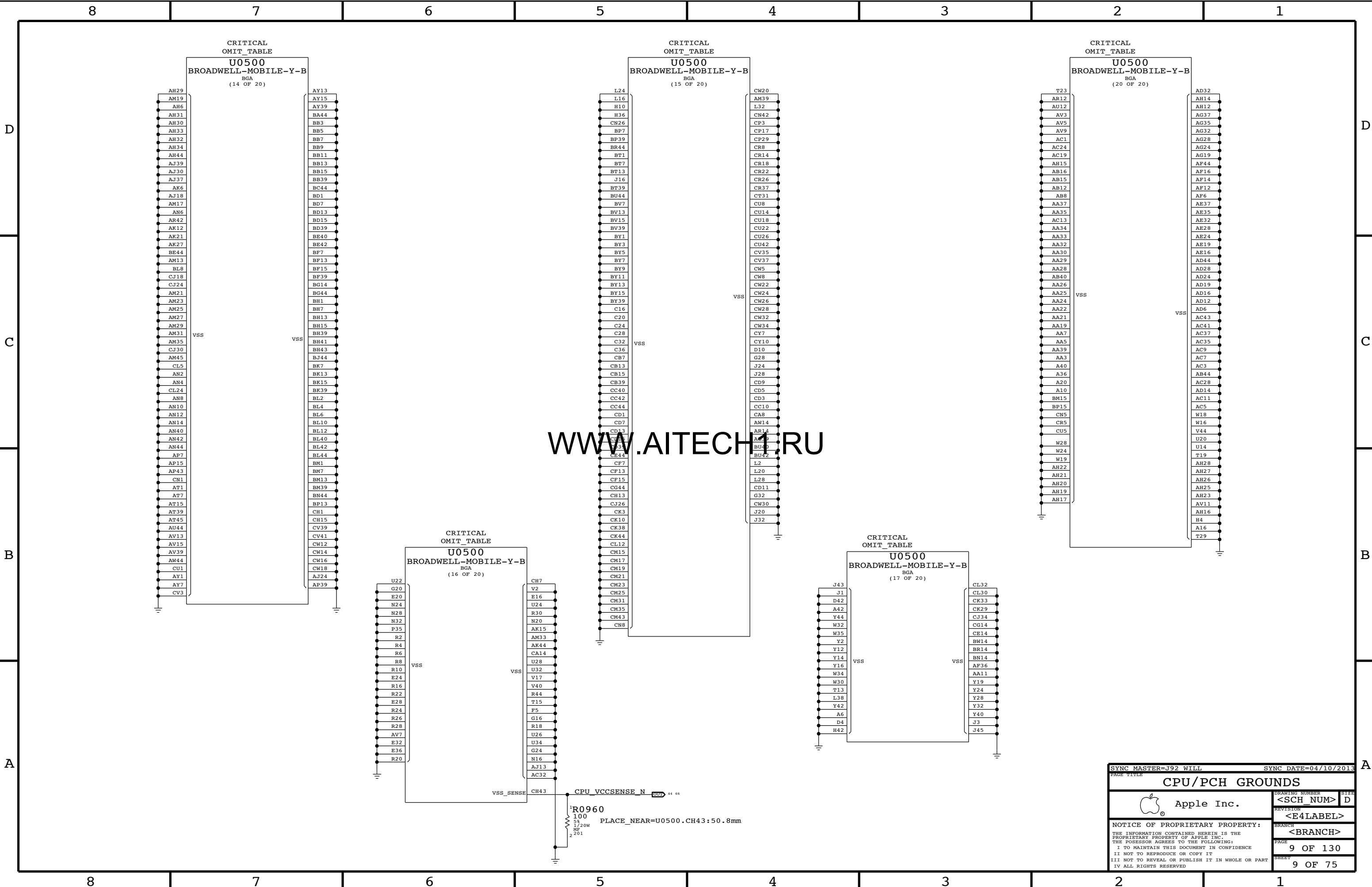
CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE
CFG<9>:NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID
CFG<8>:ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED
CFG<4>:eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG<1>:PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE
CFG<0>:RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK







SYNC MASTER=J92 DEVM1B		SYNC DATE=10/01/2013	
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CPU/PCH POWER			
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SYNC DATE=04/10/2013

CPU/PCH GROUNDS

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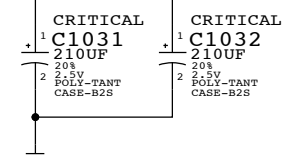
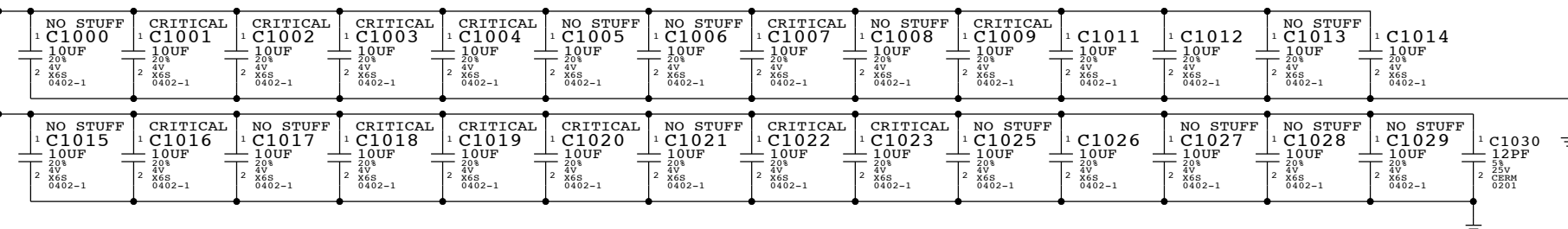
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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 0.9 unless stated otherwise

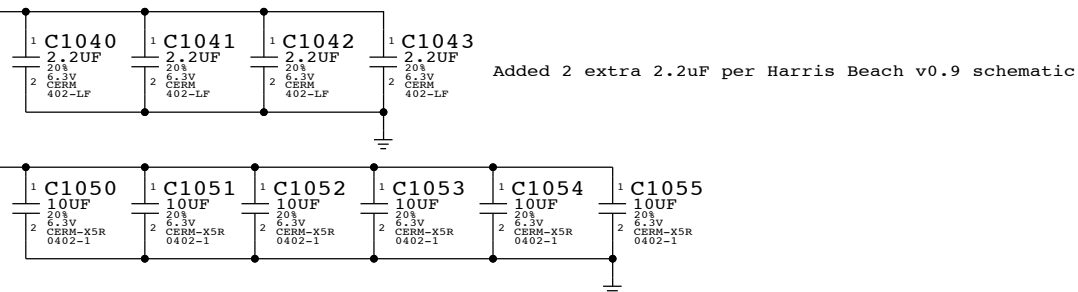
CPU VCC Decoupling

Intel recommendation (Table 5-1):	23x 22uF 0805 stuff,	7x 22uF 0805 nostuff
Apple implementation	: 16x 10uF 0402 stuff,	12x 10uF 0402 nostuff

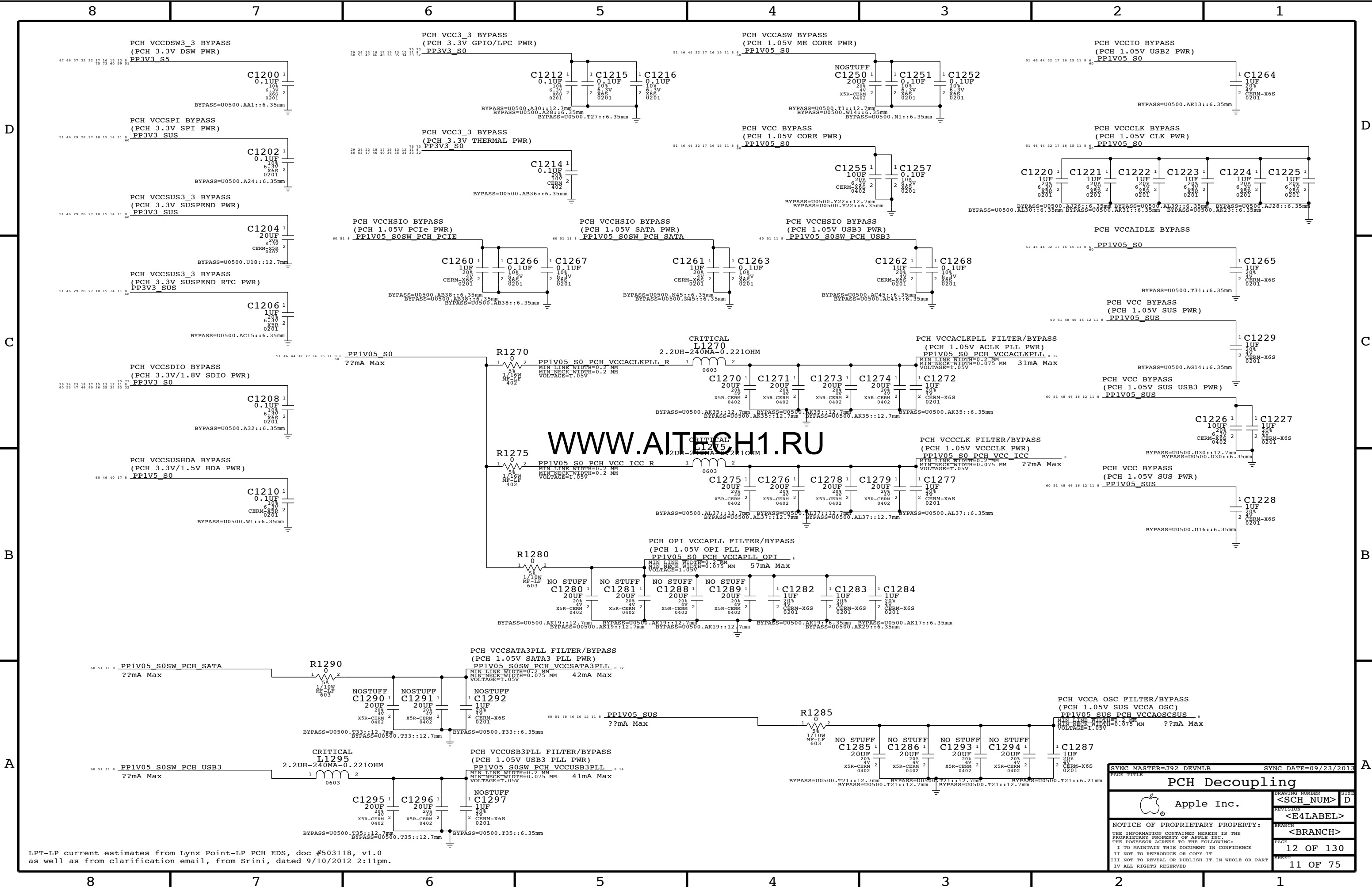


CPU VDDQ DECOUPLING


Intel recommendation (Table 5-4):	2x 2.2uF 0402, 6x 10uF 0603
Apple implementation	: 2x 2.2uF 0402, 6x 10uF 0402

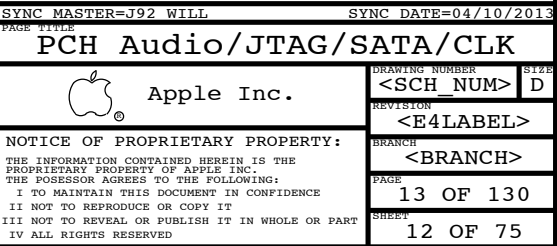


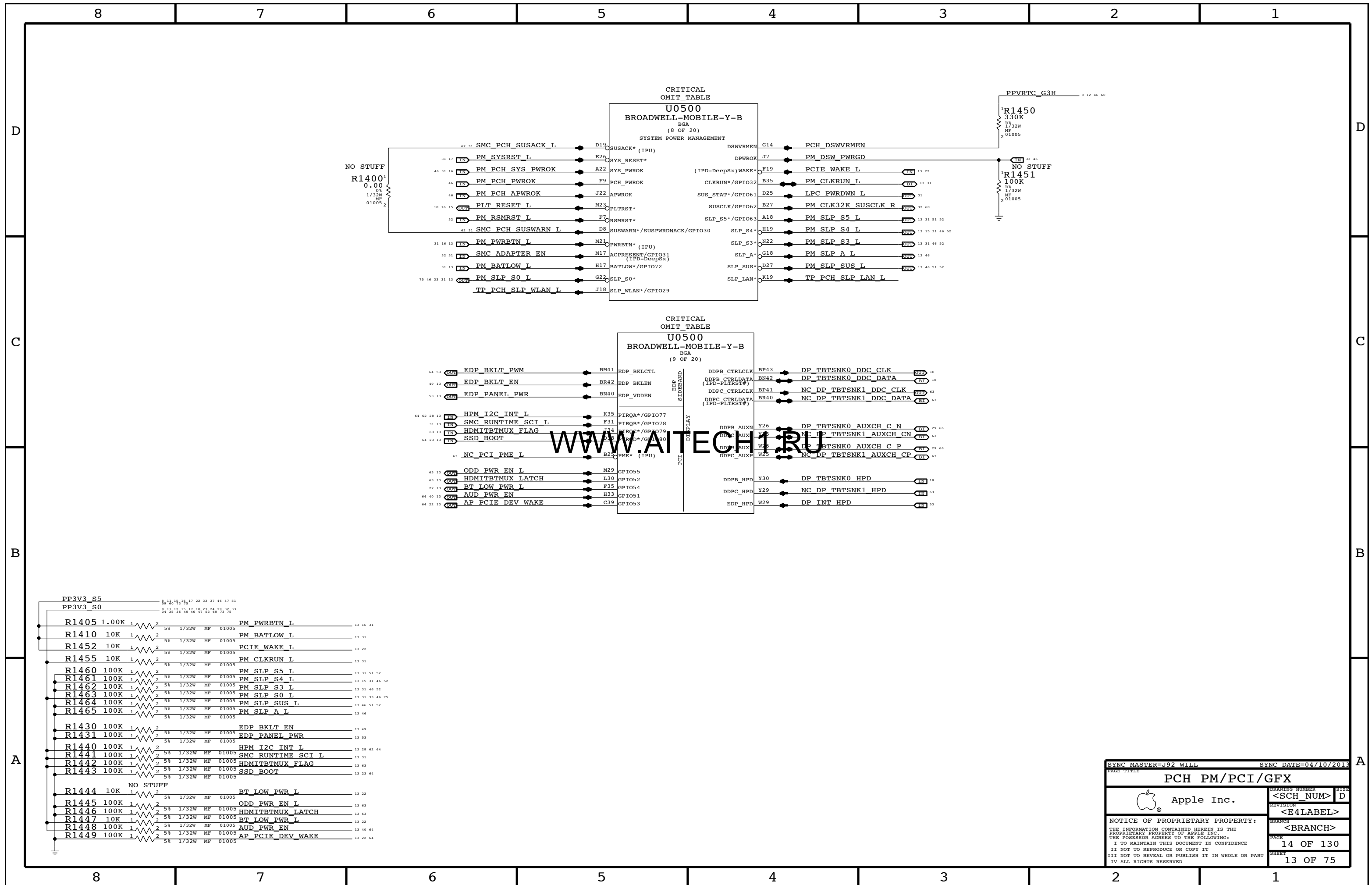
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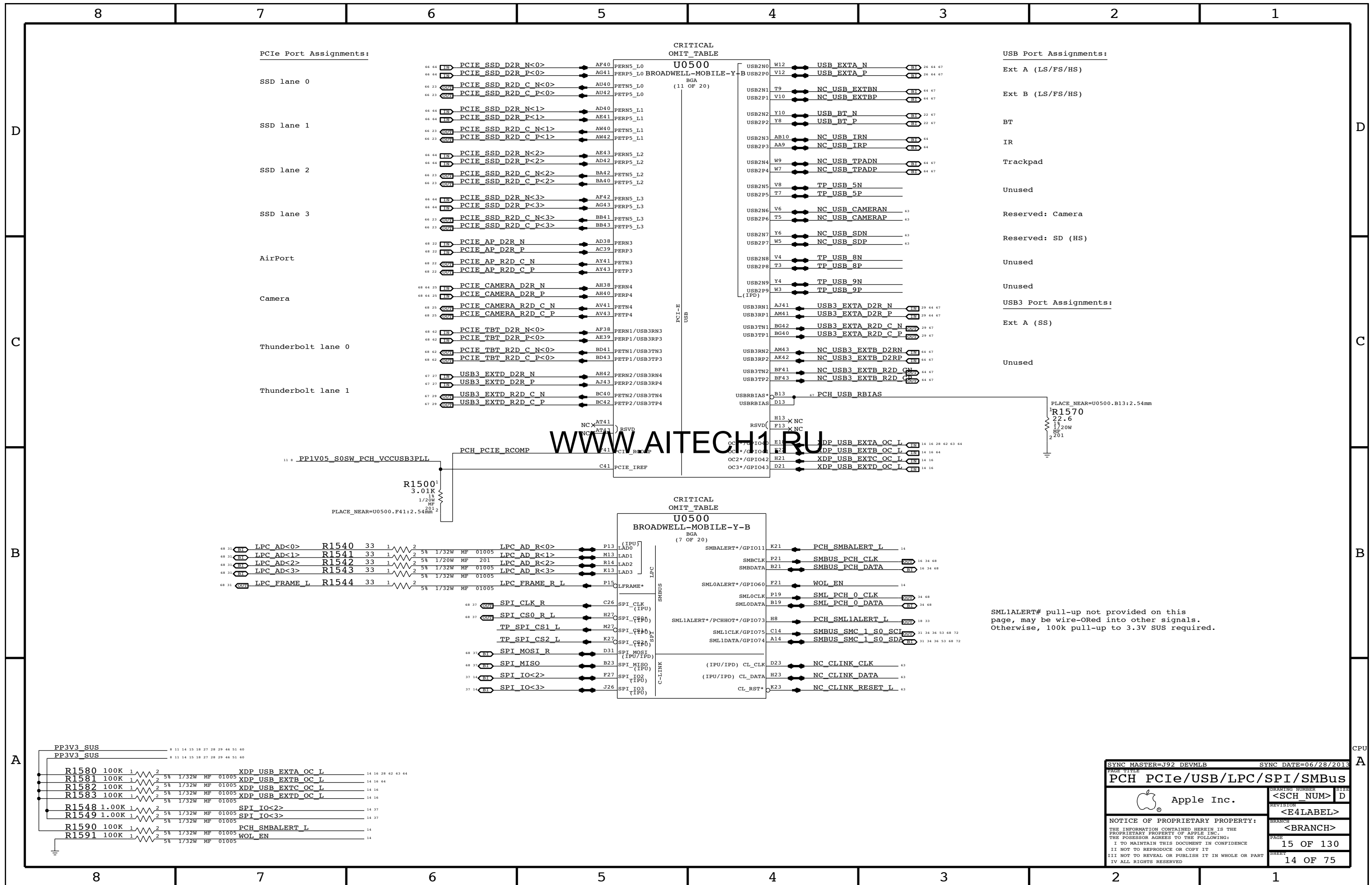


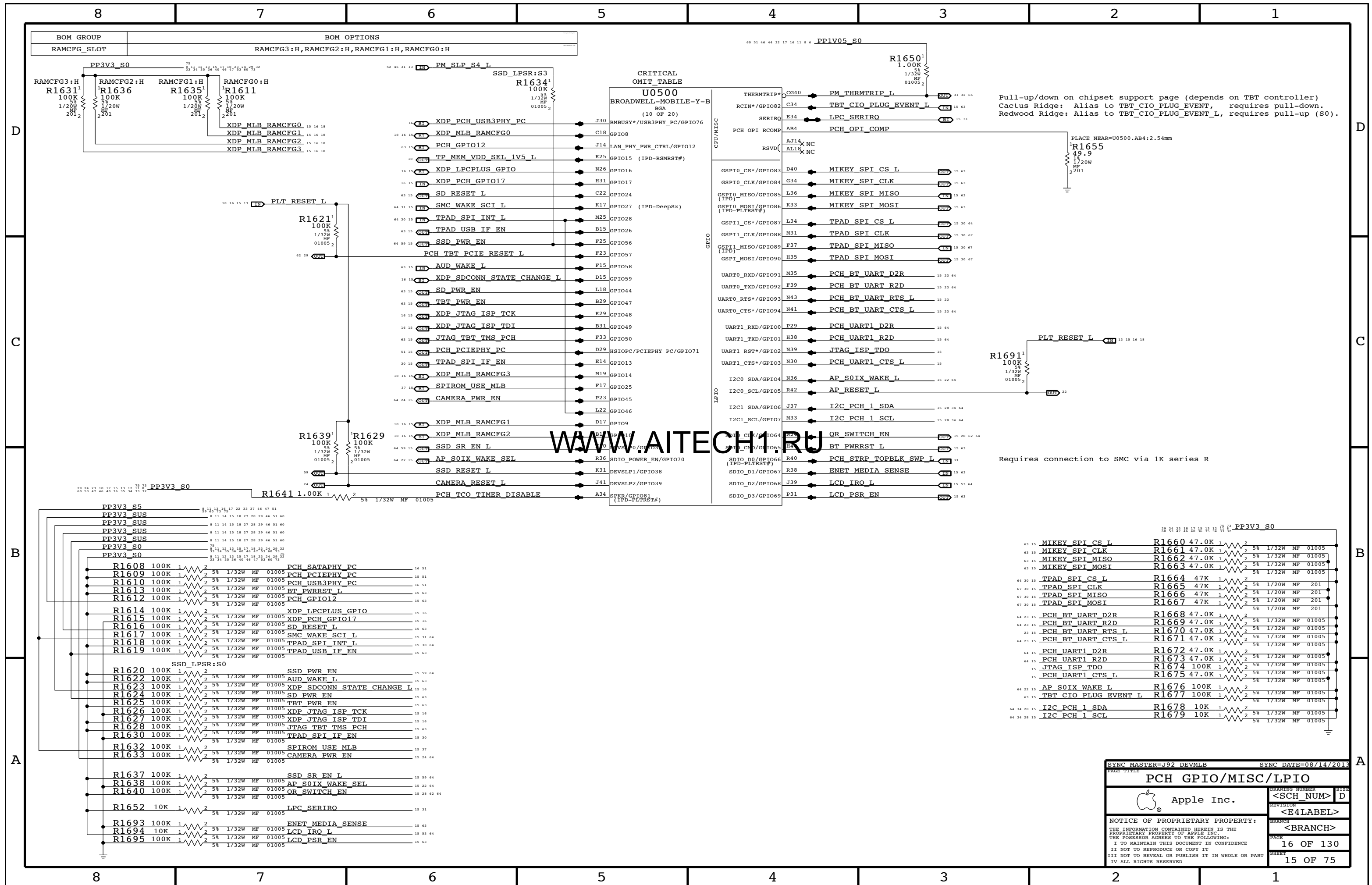
LPT-LP current estimates from Lynx Point-LP PCH EDS, doc #503118, v1.0
as well as from clarification email, from Srin, dated 9/10/2012 2:11pm.

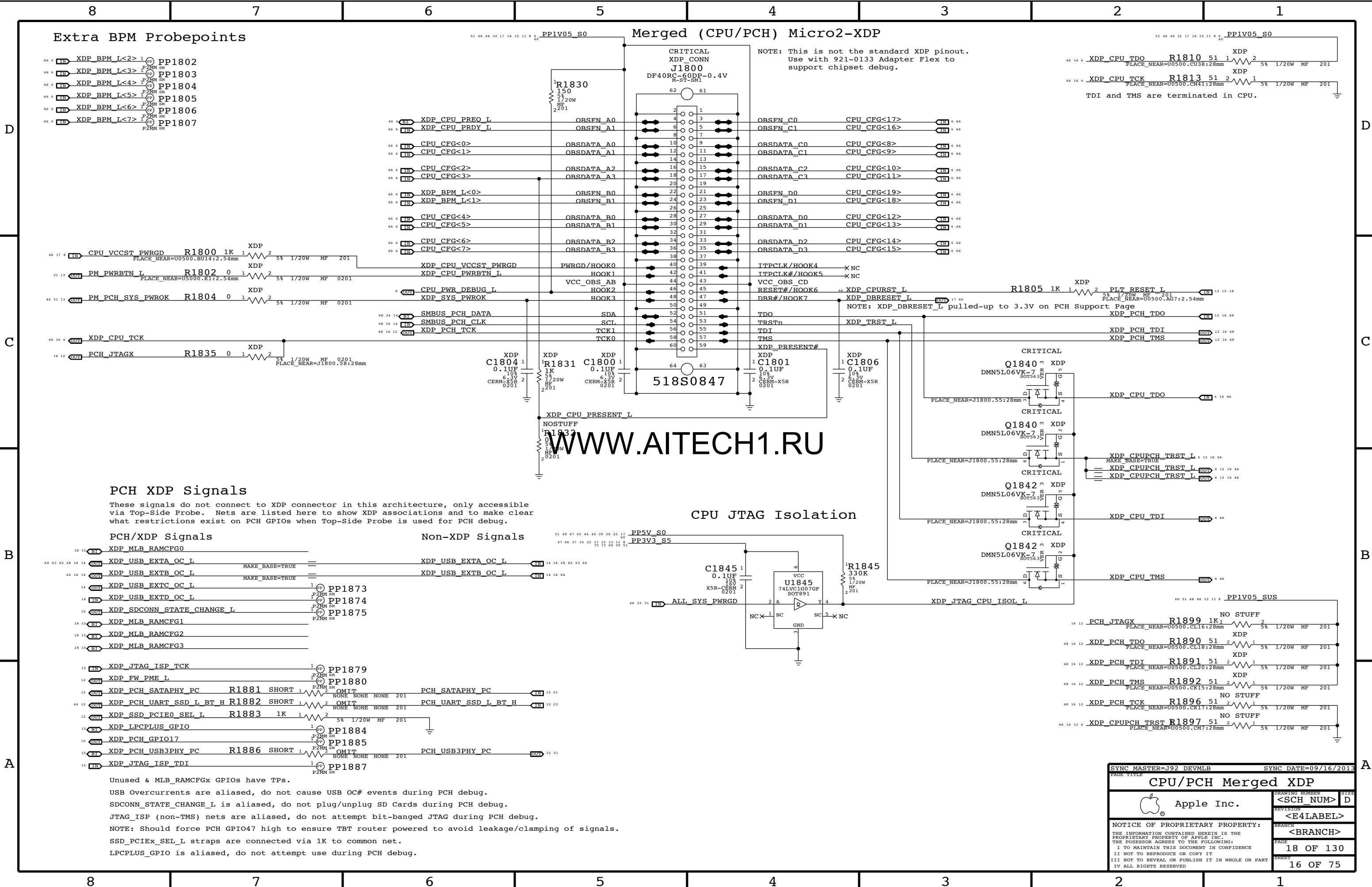
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PCH Decoupling			
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		BRANCH <BRANCH>	
		PAGE 12 OF 130	
		SHEET 11 OF 75	











Extra BPM Probepoints

- XDP_BPM_L<2> PP1802
- XDP_BPM_L<3> PP1803
- XDP_BPM_L<4> PP1804
- XDP_BPM_L<5> PP1805
- XDP_BPM_L<6> PP1806
- XDP_BPM_L<7> PP1807

Merged (CPU/PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05_S0

- XDP_CPU_TDO R1810 51 1 XDP
- XDP_CPU_TCK R1813 51 2 XDP
- TDI and TMS are terminated in CPU.

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals

- XDP_MLB_RAMCFG0
- XDP_USB_EXT_A_OC_L
- XDP_USB_EXT_B_OC_L
- XDP_USB_EXT_C_OC_L
- XDP_USB_EXT_D_OC_L
- XDP_SDCONN_STATE_CHANGE_L
- XDP_MLB_RAMCFG1
- XDP_MLB_RAMCFG2
- XDP_MLB_RAMCFG3

Non-XDP Signals

- XDP_USB_EXT_A_OC_L
- XDP_USB_EXT_B_OC_L
- XDP_USB_EXT_C_OC_L
- XDP_USB_EXT_D_OC_L
- XDP_SDCONN_STATE_CHANGE_L
- XDP_MLB_RAMCFG0
- XDP_MLB_RAMCFG1
- XDP_MLB_RAMCFG2
- XDP_MLB_RAMCFG3
- XDP_JTAG_ISP_TCK
- XDP_FW_PME_L
- XDP_PCH_SATAPHY_PC
- XDP_PCH_UART_SSD_L_BT_H
- XDP_SSD_PCIE0_SEL_L
- XDP_LPCPLUS_GPIO
- XDP_PCH_GPIO17
- XDP_PCH_USB3PHY_PC
- XDP_JTAG_ISP_TDI

Unused & MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

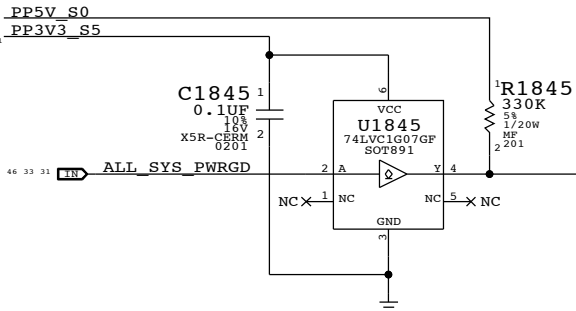
JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.


NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

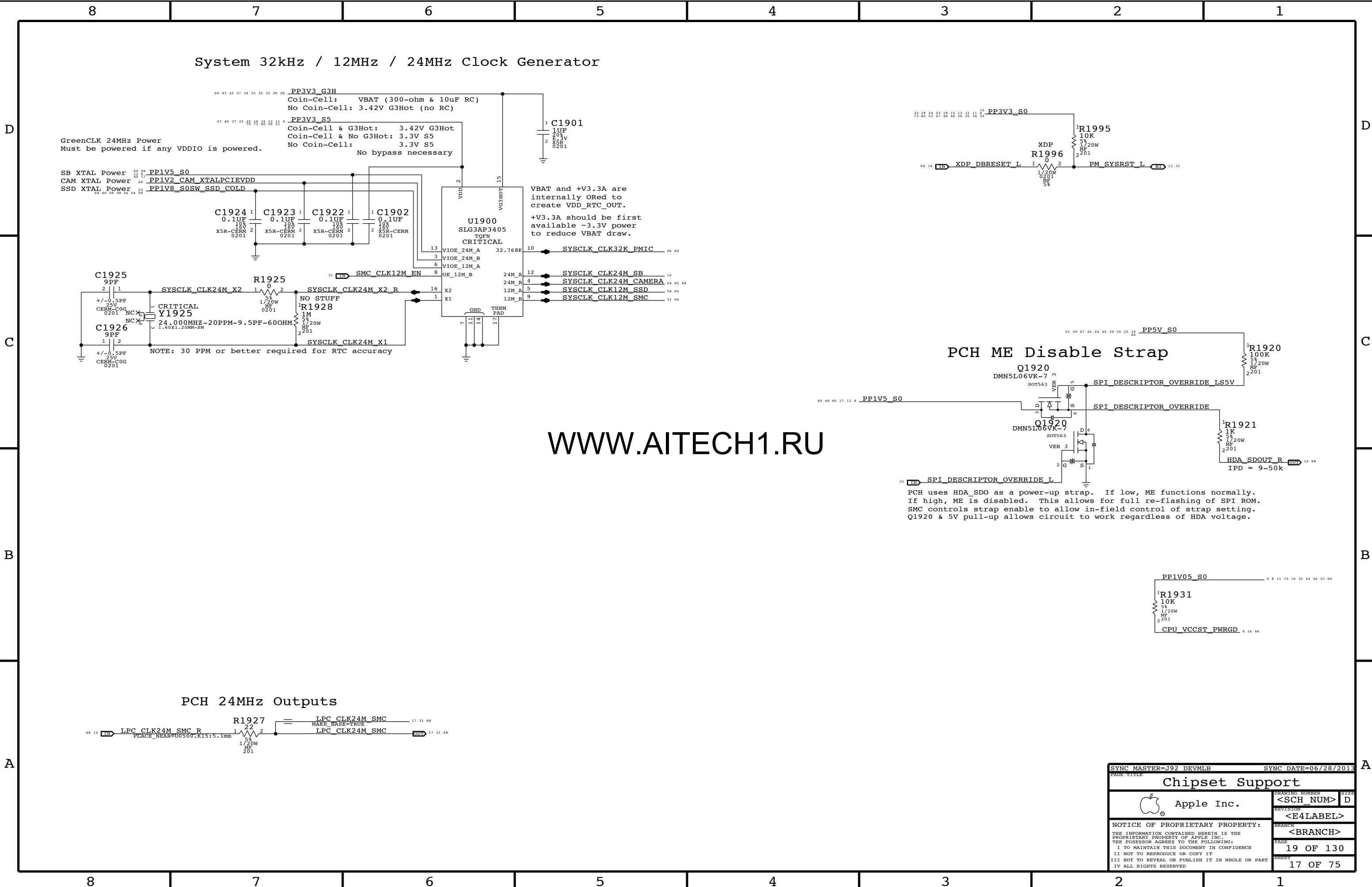
SSD_PCIEx_SEL_L straps are connected via 1K to common net.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.


CPU JTAG Isolation

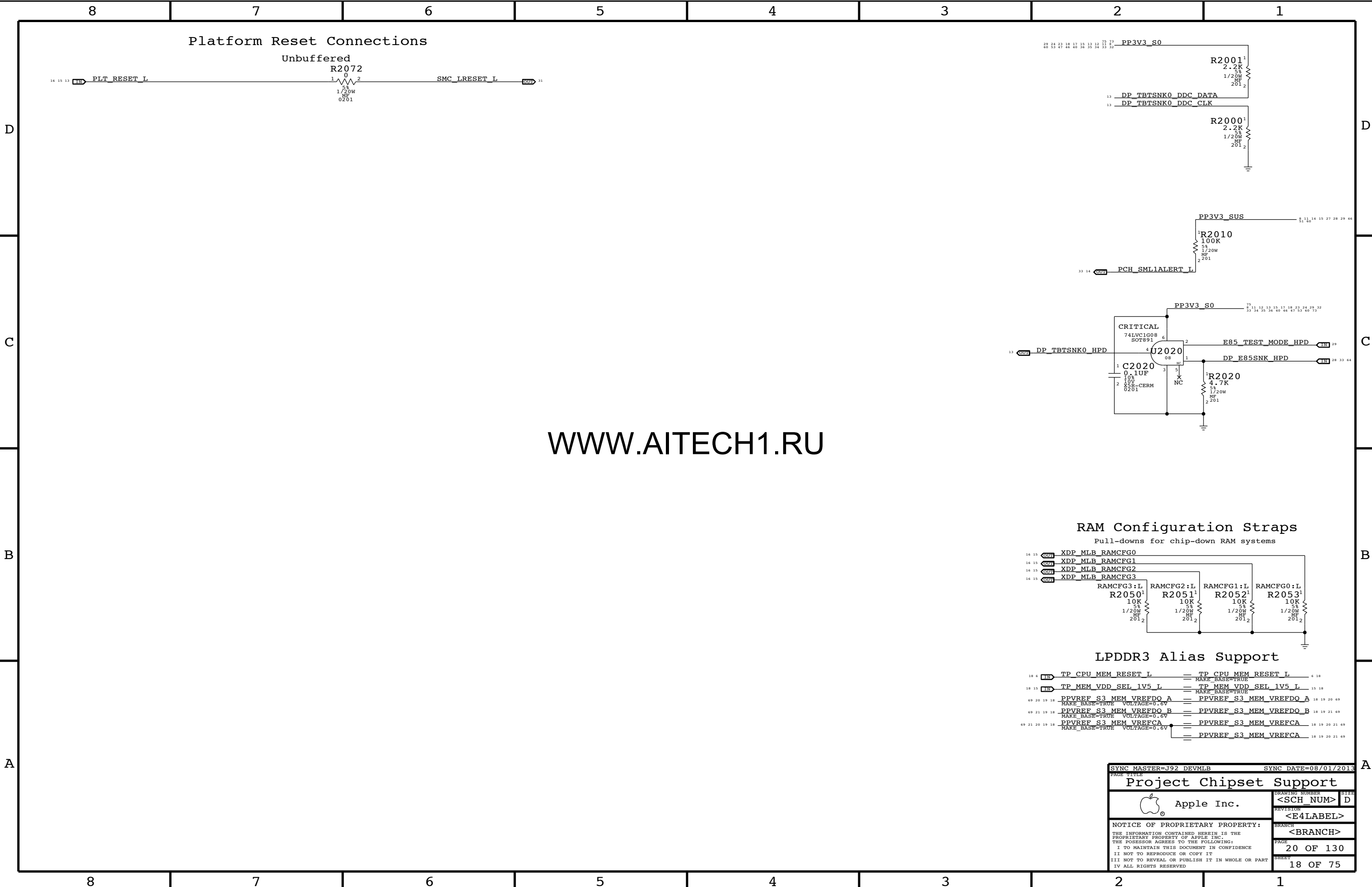


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		PAGE	18 OF 130
		SHEET	16 OF 75



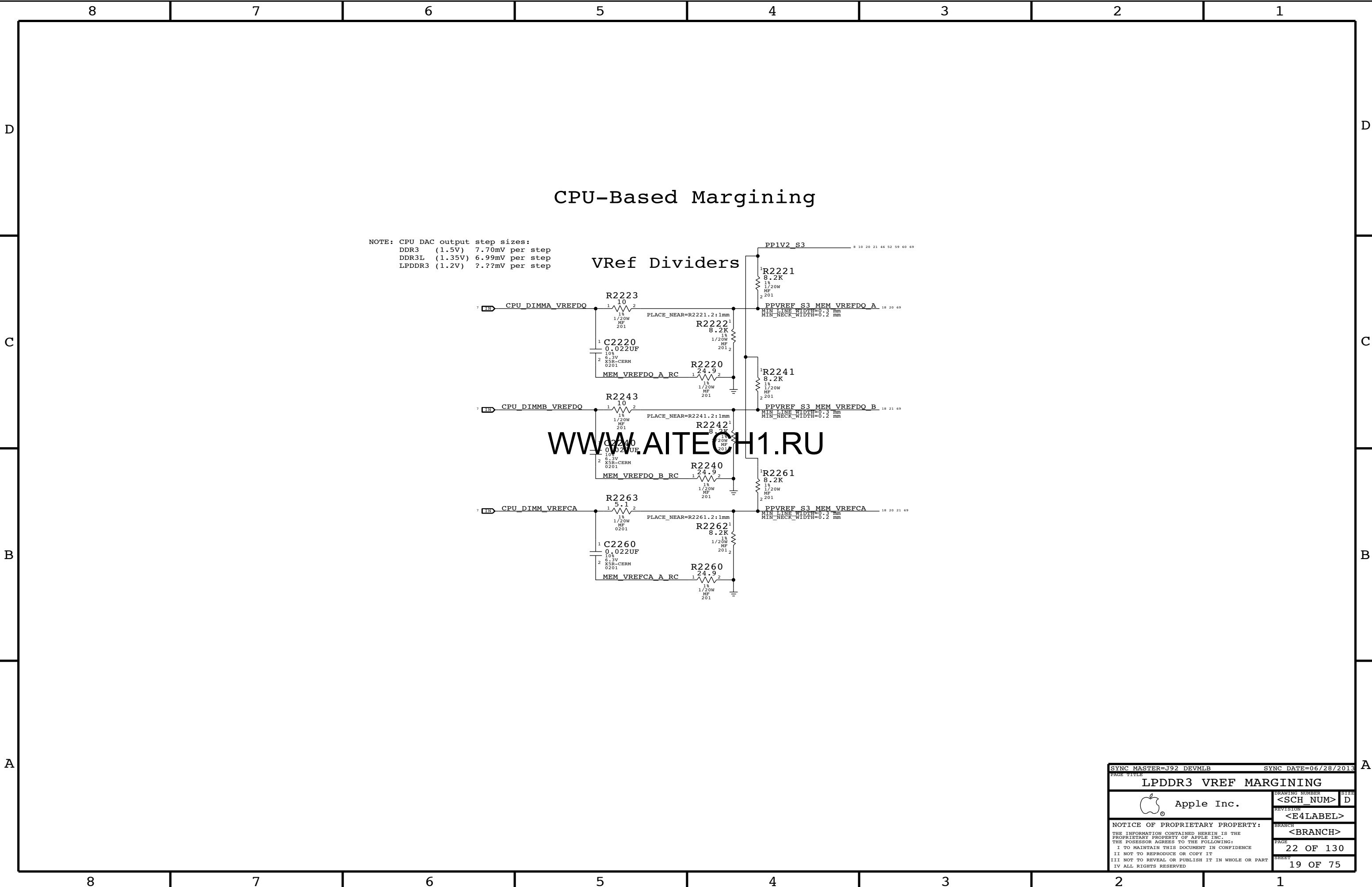
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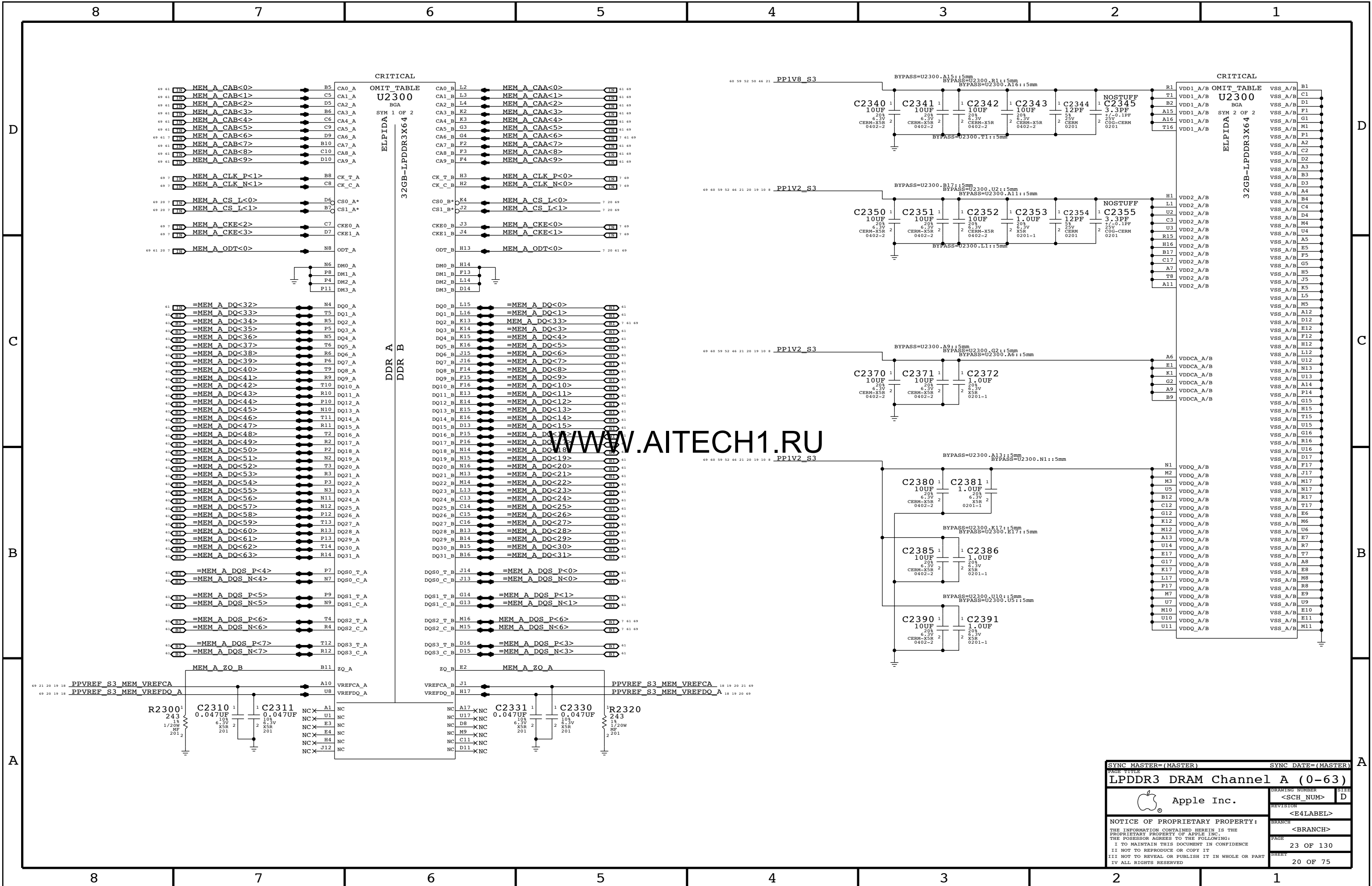
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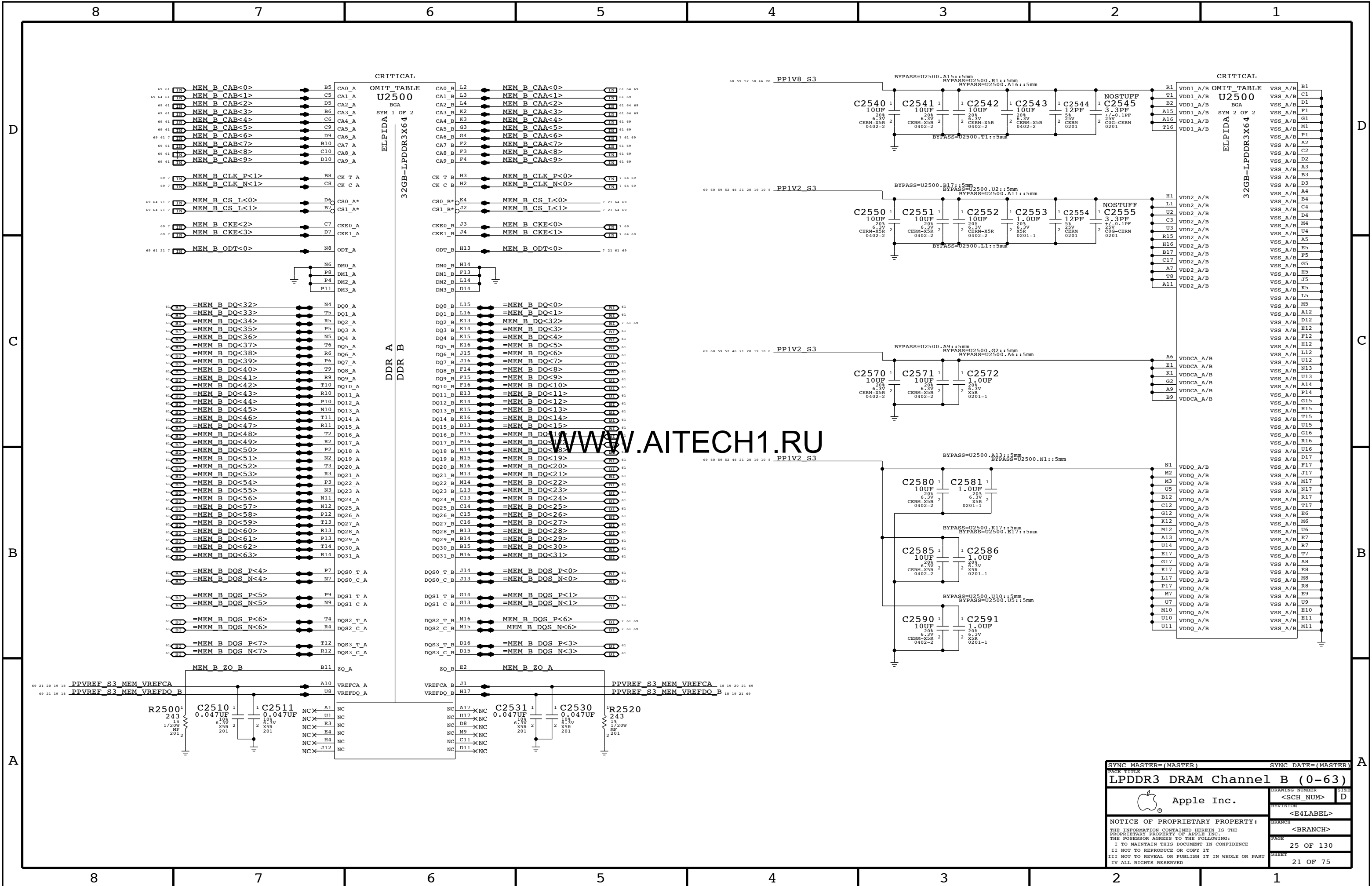
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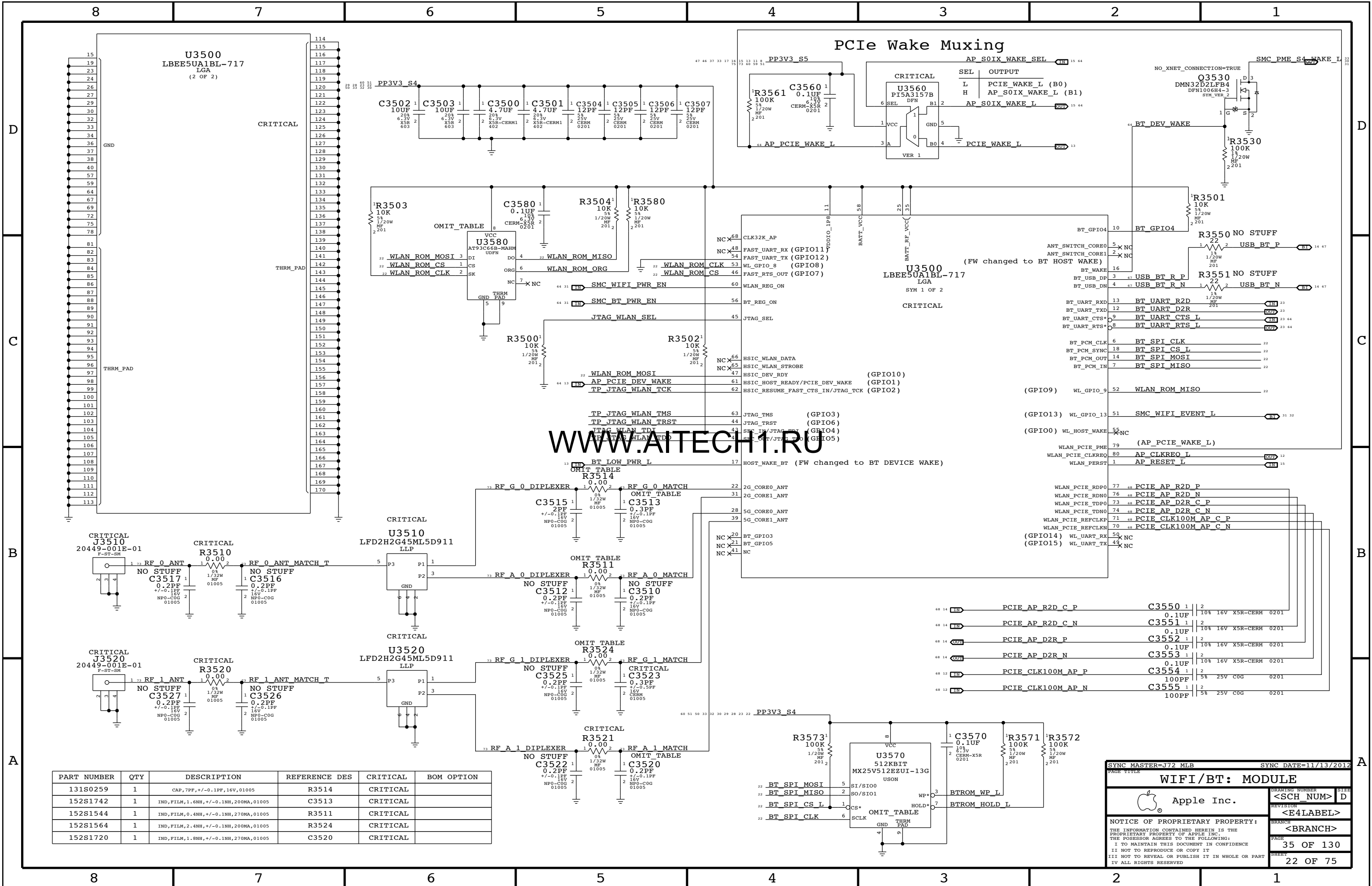
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LPDDR3 DRAM Channel A (0-63)			
 Apple Inc.	DRAWING NUMBER		SIZE
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	REVISION		
	<E4LABEL>		
BRANCH			
<BRANCH>			
PAGE			
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S0259	1	CAP, 7PF, +/-0.1PF, 16V, 01005	R3514	CRITICAL	
152S1742	1	IND, FILM, 1.6NH, +/-0.1NH, 200MA, 01005	C3513	CRITICAL	
152S1544	1	IND, FILM, 0.4NH, +/-0.1NH, 270MA, 01005	R3511	CRITICAL	
152S1564	1	IND, FILM, 2.4NH, +/-0.1NH, 200MA, 01005	R3524	CRITICAL	
152S1720	1	IND, FILM, 1.8NH, +/-0.1NH, 270MA, 01005	C3520	CRITICAL	

SYNC MASTER=J72 MLB

SYNC DATE=11/13/2012

PAGE TITLE

WIFI/BT: MODULE

 Apple Inc.

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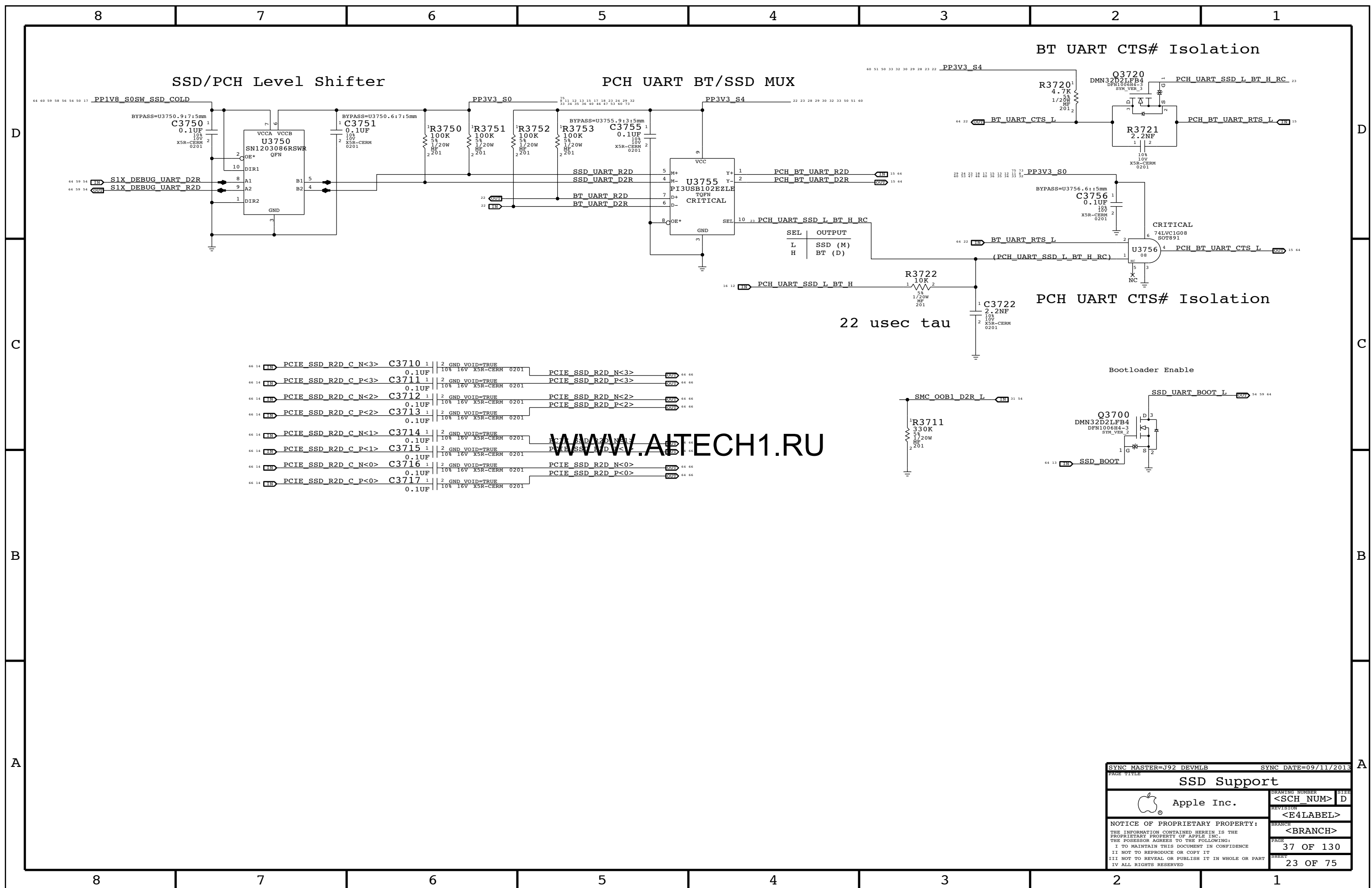
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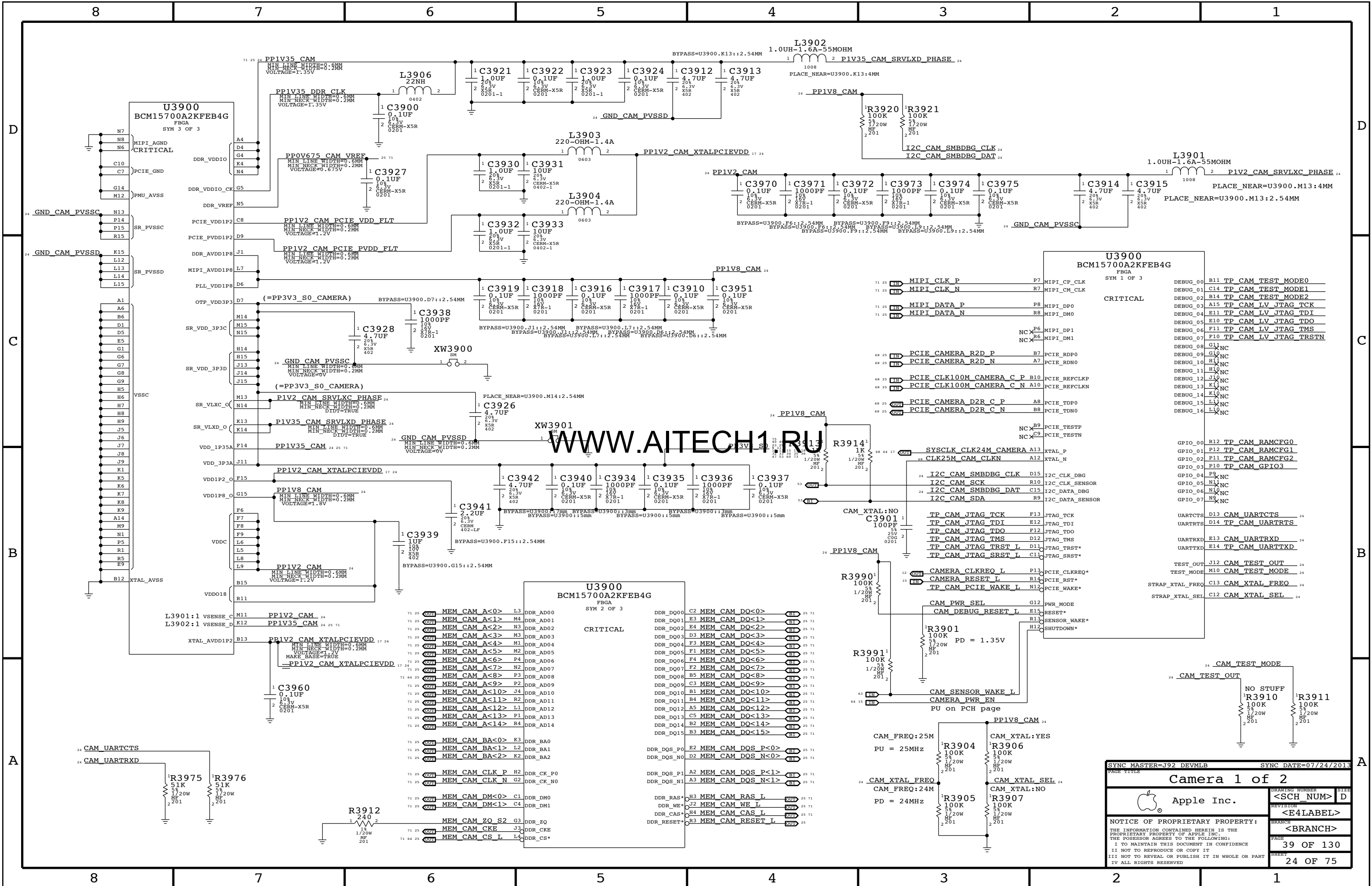
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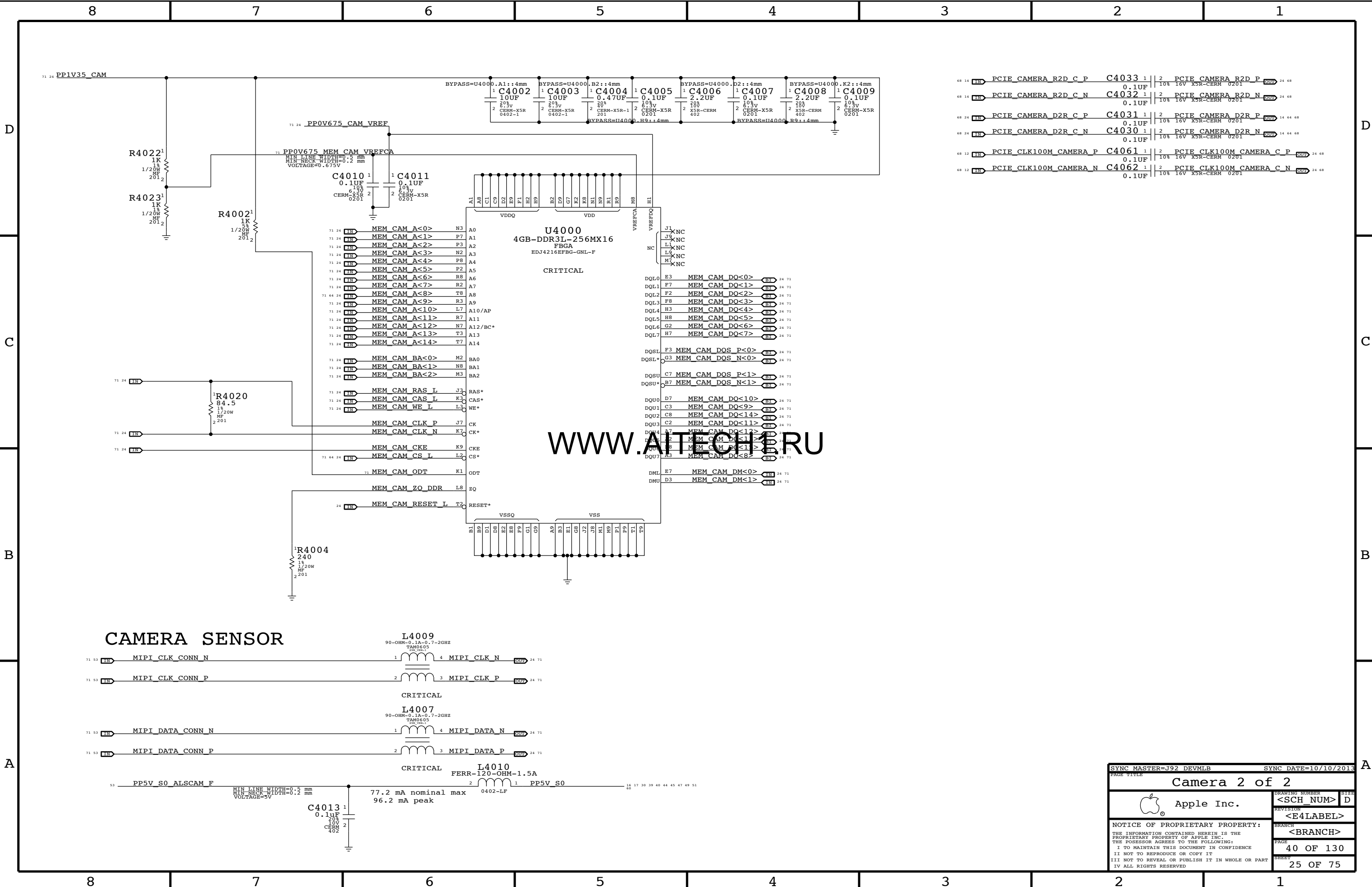
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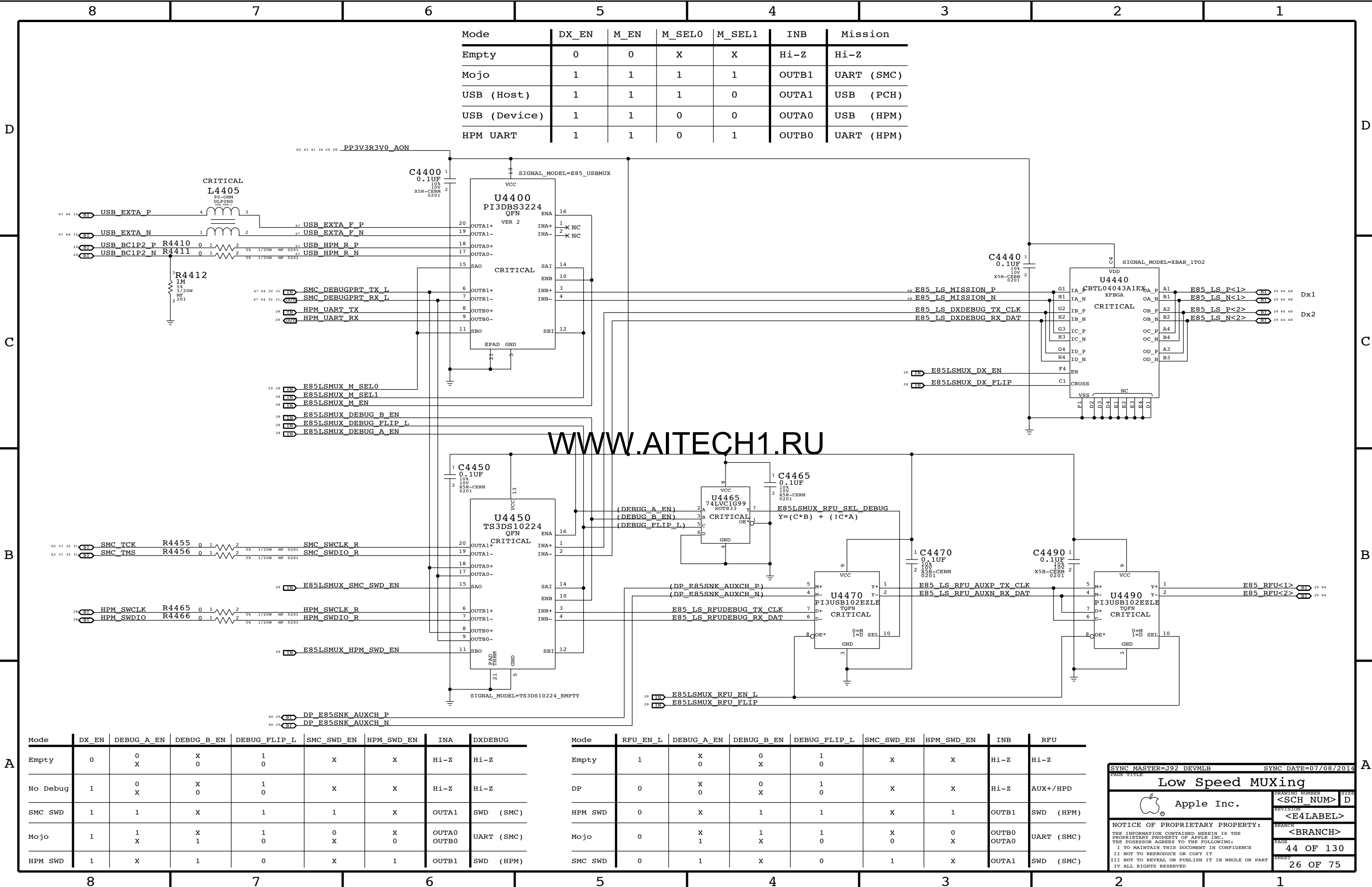
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Mode	DX_EN	M_EN	M_SEL0	M_SEL1	INB	Mission
Empty	0	0	X	X	Hi-Z	Hi-Z
Mojo	1	1	1	1	OUTB1	UART (SMC)
USB (Host)	1	1	1	0	OUTA1	USB (PCH)
USB (Device)	1	1	0	0	OUTA0	USB (HPM)
HPM UART	1	1	0	1	OUTB0	UART (HPM)

Mode	DX_EN	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INA	DXDEBUG
Empty	0	0	X	0	X	X	Hi-Z	Hi-Z
No Debug	1	0	X	0	X	X	Hi-Z	Hi-Z
SMC SWD	1	1	X	1	1	X	OUTA1	SWD (SMC)
Mojo	1	1	X	1	0	X	OUTA0 OUTB0	UART (SMC)
HPM SWD	1	X	1	0	X	1	OUTB1	SWD (HPM)

Mode	RFU_EN_L	DEBUG_A_EN	DEBUG_B_EN	DEBUG_FLIP_L	SMC_SWD_EN	HPM_SWD_EN	INB	RFU
Empty	1	X	0	0	X	X	Hi-Z	Hi-Z
DP	0	X	0	0	X	X	Hi-Z	AUX+/HPD
HPM SWD	0	X	1	1	X	1	OUTB1	SWD (HPM)
Mojo	0	X	1	0	X	0	OUTB0 OUTA0	UART (SMC)
SMC SWD	0	1	X	0	1	X	OUTA1	SWD (SMC)

SYNC MASTER=J92 DEVMLB

SYNC DATE=07/08/2014

Low Speed MUXing

Apple Inc.

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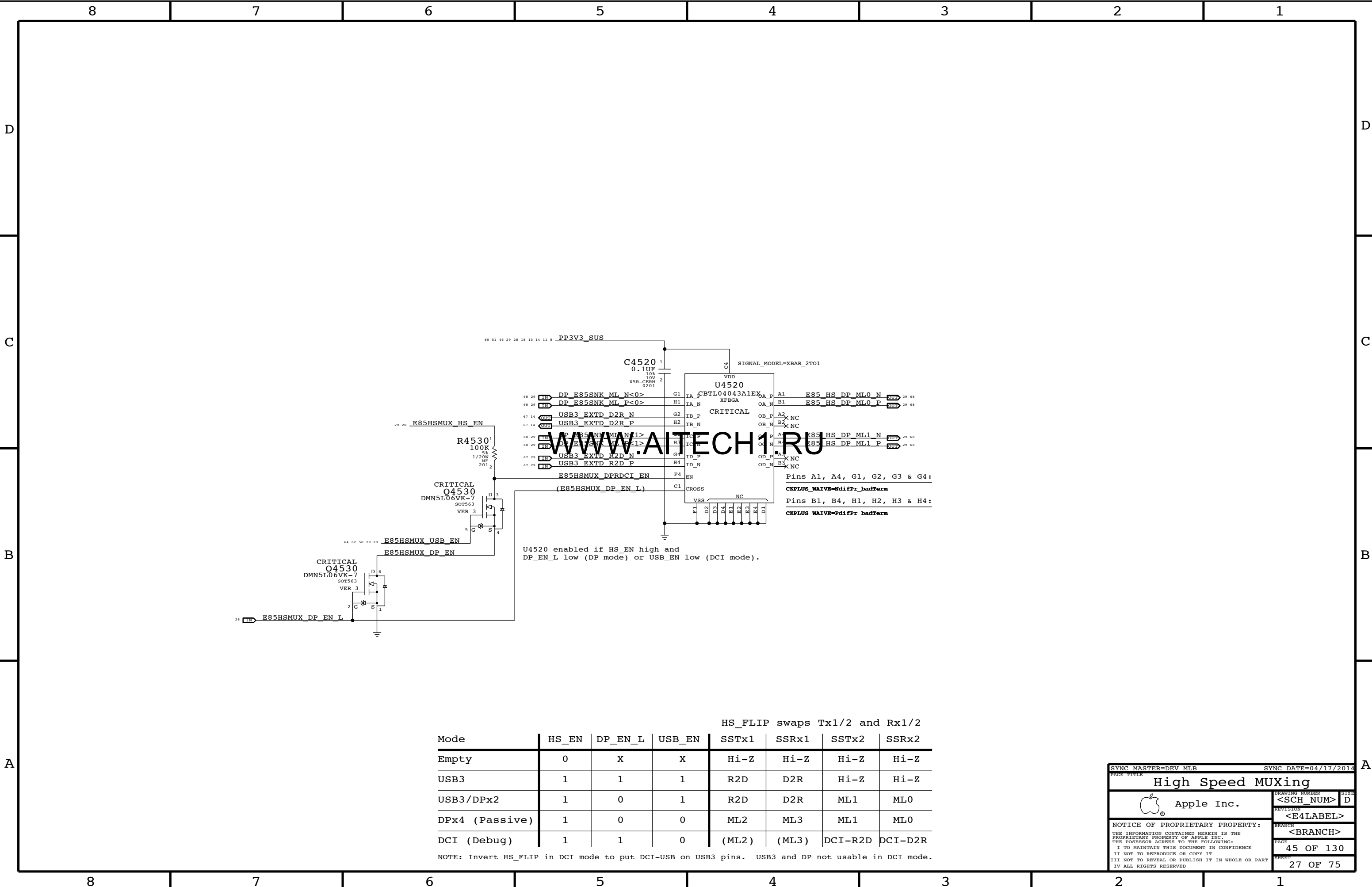
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HS_FLIP swaps Tx1/2 and Rx1/2							
Mode	HS_EN	DP_EN_L	USB_EN	SSTx1	SSRx1	SSTx2	SSRx2
Empty	0	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
USB3	1	1	1	R2D	D2R	Hi-Z	Hi-Z
USB3/DPx2	1	0	1	R2D	D2R	ML1	ML0
DPx4 (Passive)	1	0	0	ML2	ML3	ML1	ML0
DCI (Debug)	1	1	0	(ML2)	(ML3)	DCI-R2D	DCI-D2R


NOTE: Invert HS_FLIP in DCI mode to put DCI-USB on USB3 pins. USB3 and DP not usable in DCI mode.

SYNC MASTER=DEV MLB

SYNC DATE=04/17/2014

PAGE TITLE

High Speed MUXing

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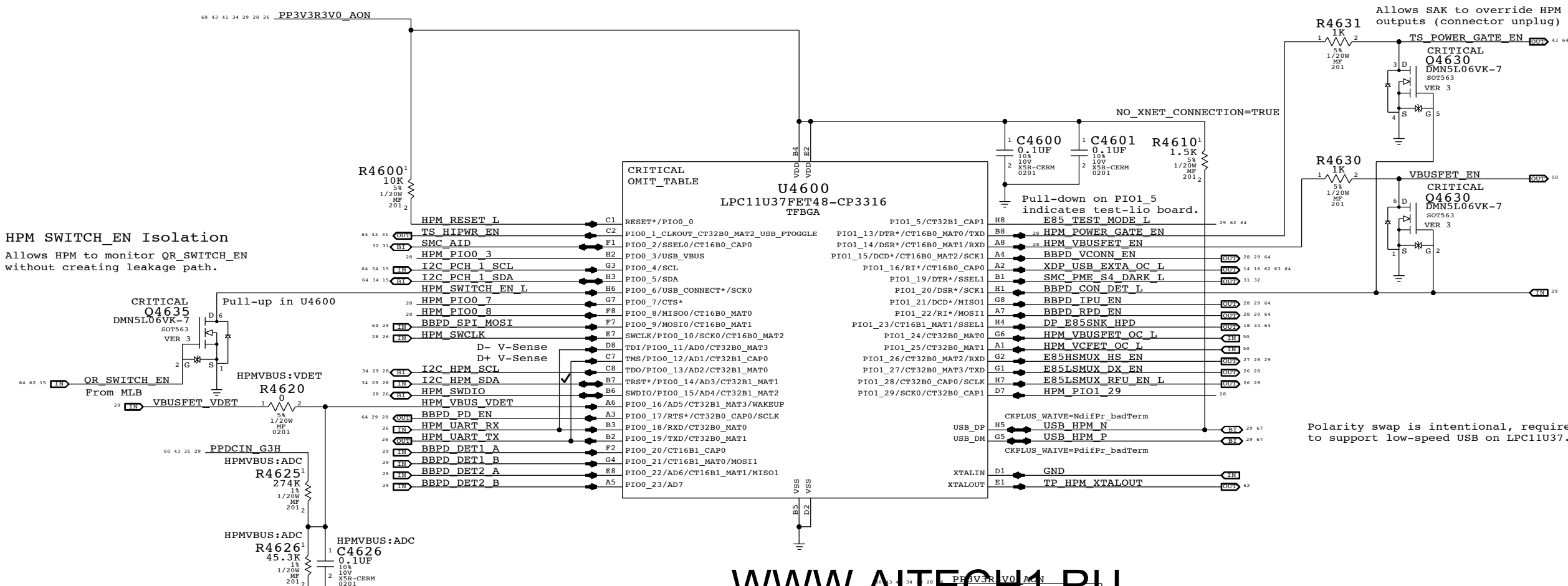
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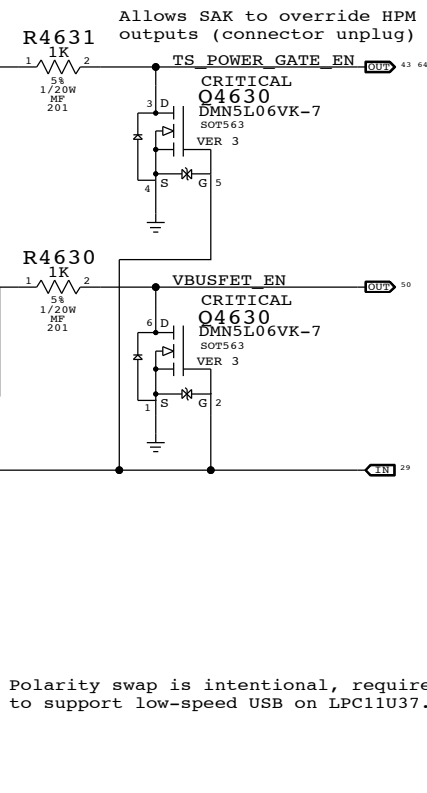
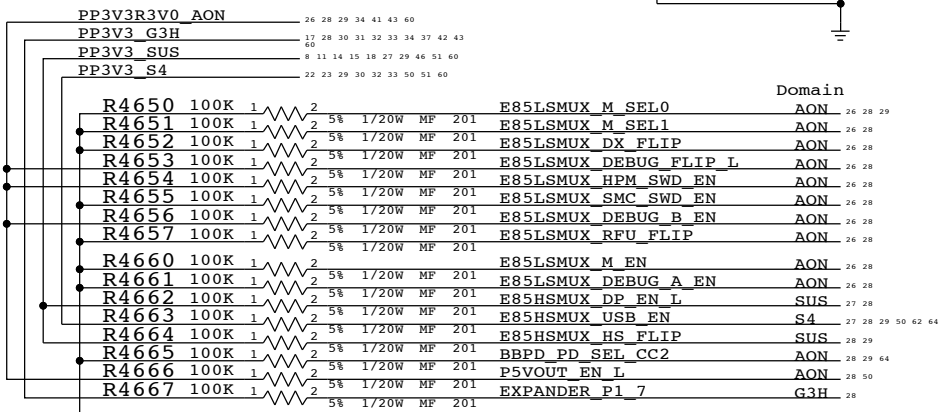
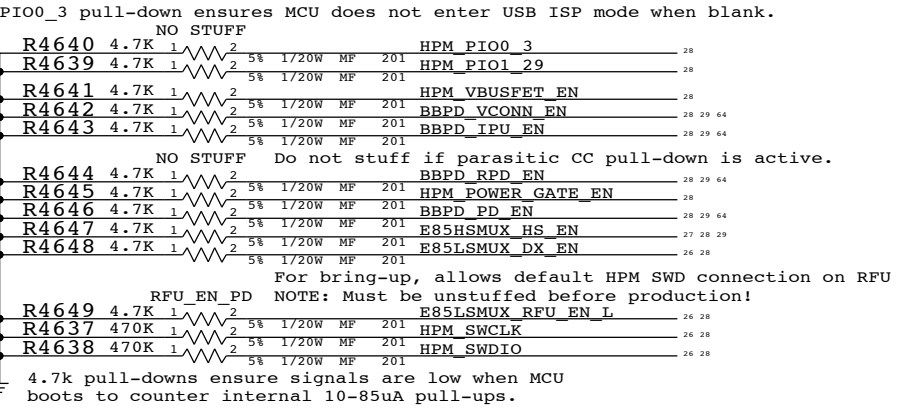
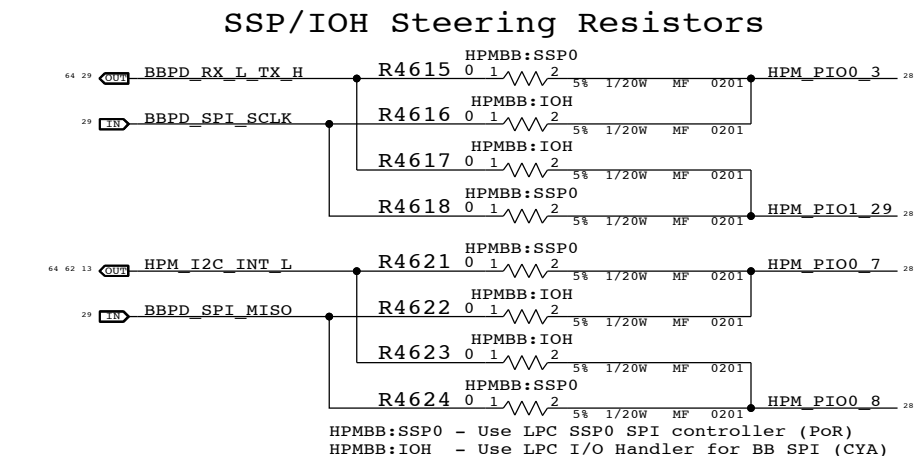
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Host Port Micro

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All non-AON signals are open-drain to avoid leakage.
P1_7 in G3H domain for initial detection of G3H power.

D

C

B

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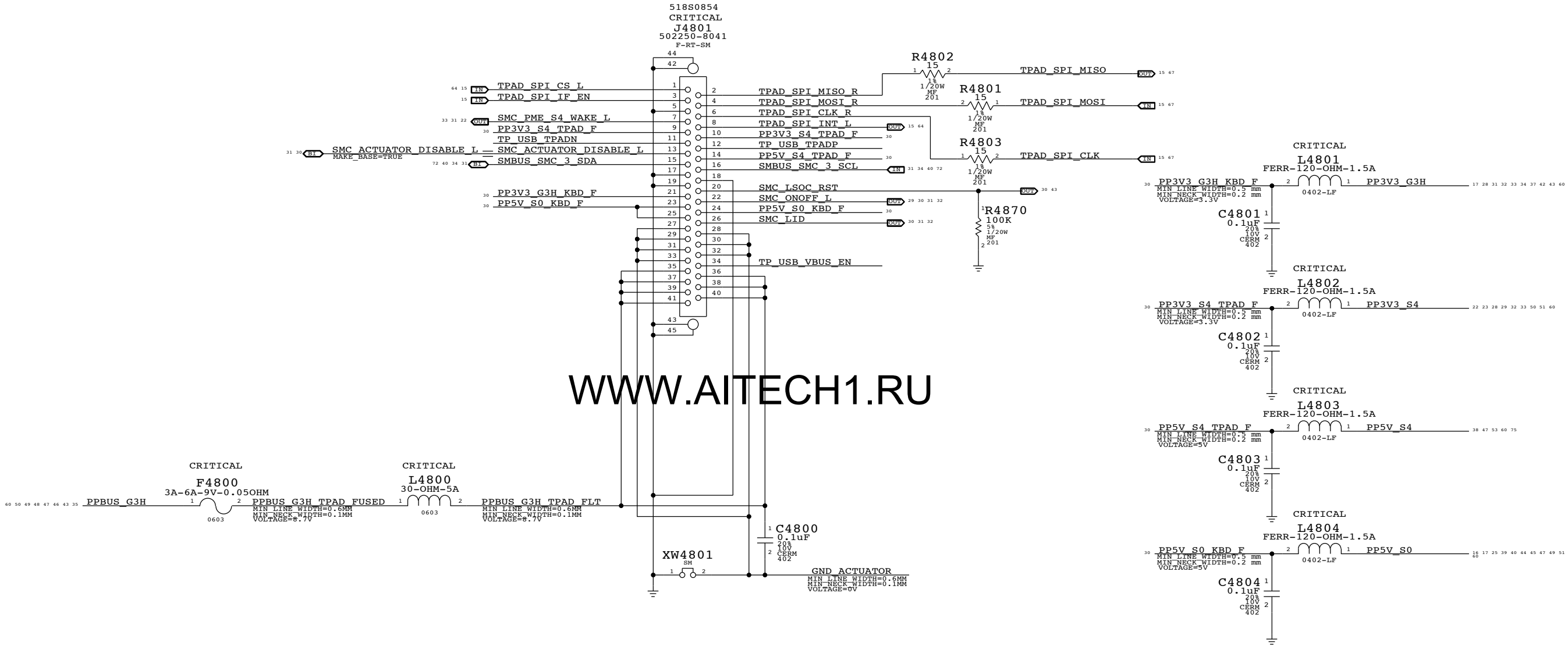
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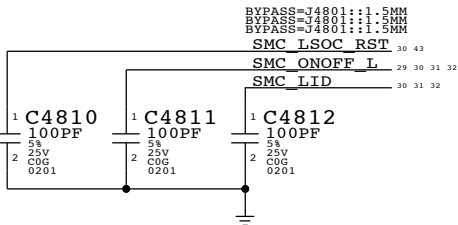
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IPD ZIF CONNECTOR

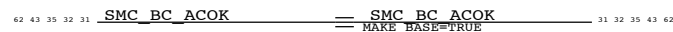
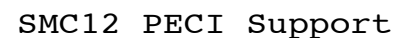
Bottom side contacts used
Pinout reversed from flex



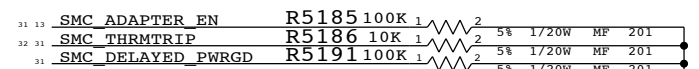
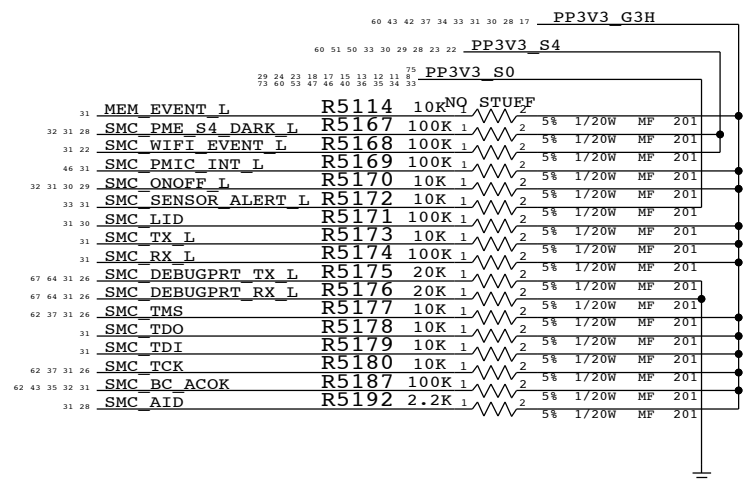
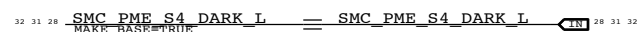
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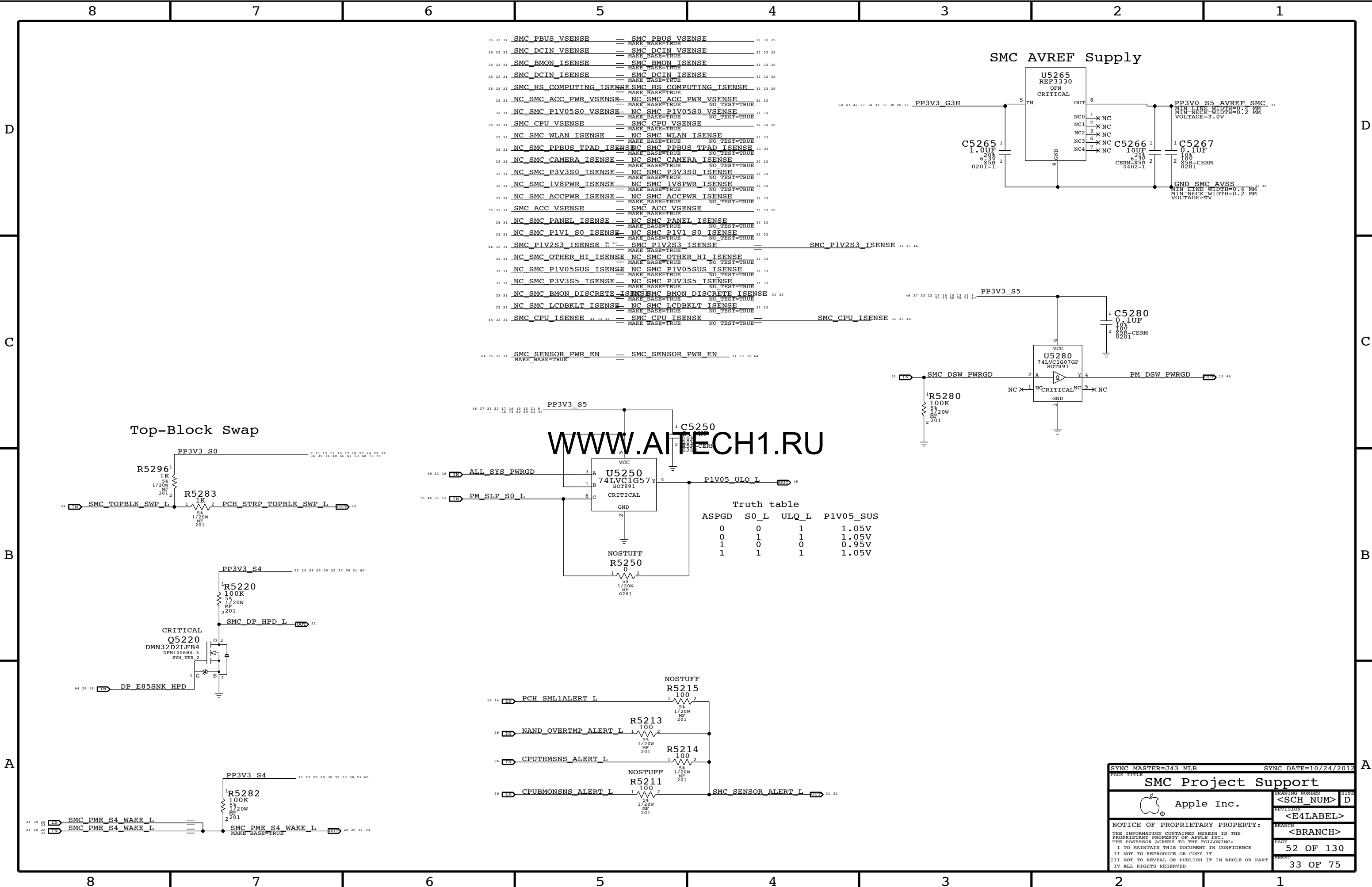


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Keyboard & Trackpad Conn			
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C

A



Top-Block Swap

SMC AVREF Supply


Truth table

ASPGD	S0_L	ULQ_L	PIV05_SUS
0	0	1	1.05V
0	1	1	1.05V
1	0	0	0.95V
1	1	1	1.05V

SYNC MASTER=J43 MLB

SYNC DATE=10/24/2012

SMC Project Support

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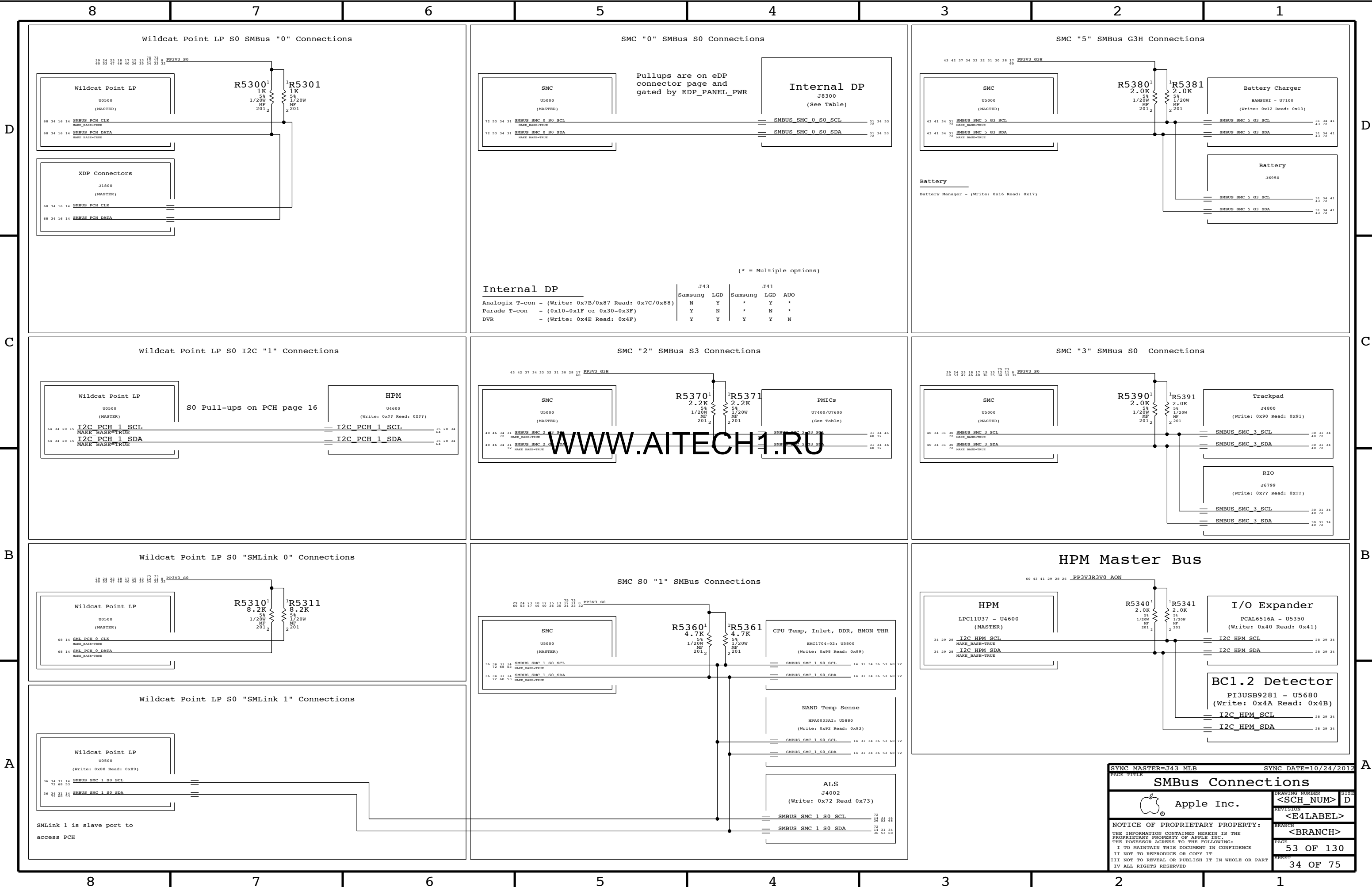
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POR VOLTAGE / CURRENT SENSORS : TO BE USED IN PRODUCTION

VP0R: PBUS Voltage Sense Enable & Filter

IC0R : COMPUTING High Side Current Sense

Need to set gains for ULX

EMC1704 Computing High Side Gain Stage

VD0R: DC-In Voltage Sense Enable & Filter

CHARGER BMON High Side Current Sense

DC-IN (AMON) Current Sense

VCFR CPU Vcore Voltage Sense / Filter

ACC Voltage Sense

WWW.AITECH1.RU

Gain: 500X

In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800. This will set the mininum current threshold at 0.100mA

SYNC MASTER=J92 DEVMLB SYNC DATE=02/07/2014

Voltage & Current Sensing

Apple Inc.

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[illegible][illegible]

CHARGER BMON High Side Current Sense

PLACE_NEAR=U0000.F2:11MM

R5420
300K

43 CHGR_BMON 1 2 SMC_BMON_ISENSE 31 33

ISL6259 Gain: 36x
Scale: 2.78A / V
Max Vout: 3.3V at 9.167A
EDP Current: 310A

1 20W HP 201

C5420
3300PF

10V

1 2 XTR-CERM 0201

GND GND GND

DC-IN (AMON) Current Sense

PLACE_NEAR=U5000.F1:110M

R5430

45 **CHGR_AMON** 1 **45.3k** **SMC_DCIN_ISENSE** **00P** 31 33

1/20W
MF
201

10V

1 **C5430**
2 **2.2NF**
10%
X5R-CERM
0201

GND_SMC_AVSS 31 33 35

Sense R is R7120, 20mOhm
ISL6259 Gain: 20x
Max VOut: 1.4V at 8.25A
Scale: 2.5A / V
EDP Current: 3.5A

IC0R : COMPUTING High Side Current Sense

EDP Current :12A
MAX Vdiff : 24 mV
GAIN : 100X

PP3V3_S0

PPBUS_S5_HS_COMPUTING_ISNS

CRITICAL

R5450 0.002

ISNS_HS_COMPUTING_N

ISNS_HS_COMPUTING_P

PPBUS_G3H

U5450 INA214 CRITICAL

IN-

IN+

REF

GND

PLACE_NEAR=U5450:5MM

BYPASS=U5450:3:5MM

C5450 0.1UF

ISNS_HS_COMPUTING_IOUT

R5455 4.53K

SMC_HS_COMPUTING_ISENSE

C5455 0.22UF

GND_SMC_AVSS

PLACEMENT_NOTES:

Place close to SMC
(For R and C)

Need to set gains for ULX	
---------------------------	--

In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

With 100mA battery current, Will have 10.2mV difference going into sense pins of U5800. This will set the minumum current threshold at 0.100mA	B
---	---

VCFR CPU Vcore Voltage Sense / Filter

60 45 10 8 PPVCC_S0_CPU

1 2 CPUVSENSE_IN

PLACE_NEAR=R7320.2:11MM

1 4 5 3K R5421

1 2 SMC_CPU_VSENSE

1 2 0.22UF C5421

20V 0.22UF

6.3V 0.22UF

2 35 35 GND_SMC_AVSS


PLACE_NEAR=U5000.A4:11MM

PLACE_NEAR=U5000.A4:11MM

ACC Voltage Sense

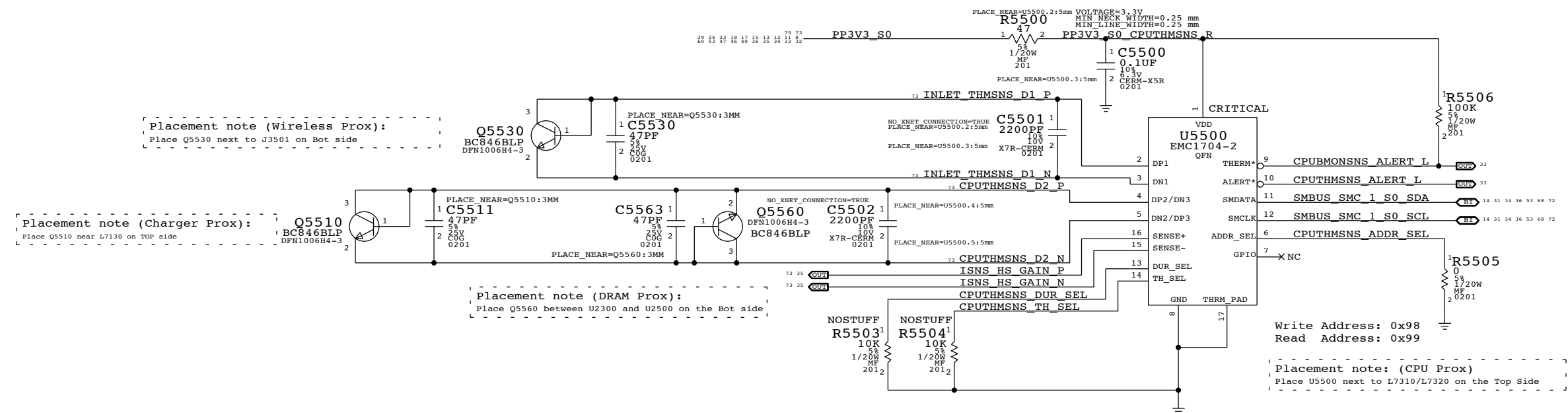
Max VOut: 3V at 5.535V Input

SYNC MASTER=J92 DEVMLB		SYNC DATE=02/07/2014	
PAGE TITLE			
Voltage & Current Sensing		DRAWING NUMBER	SIZE
Apple Inc.		<SCH_NUM>	D
REVISTOR		<E4LABEL>	
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		PAGE	54 OF 130
		SHEET	25 OF 25

SYNC MASTER=J92 DEVMLB		SYNC DATE=02/07/2014	
PAGE TITLE			
Voltage & Current Sensing			
		DRAWING NUMBER	SIZE
Apple Inc.		<SCH NUM>	D
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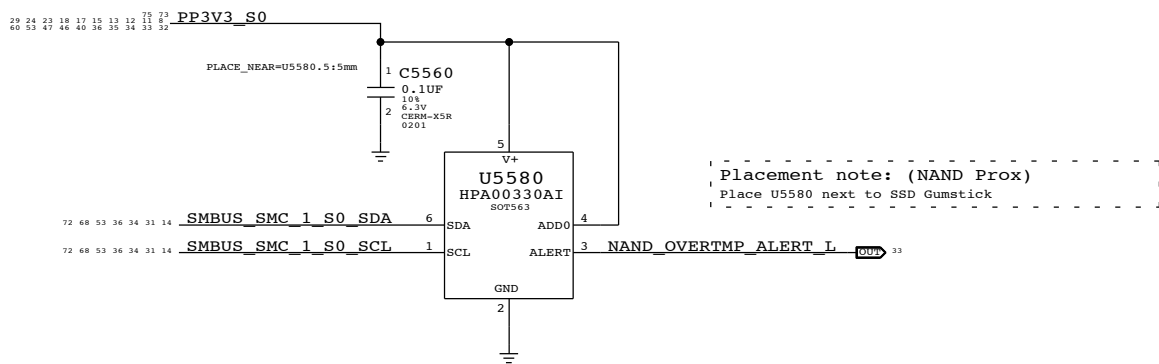
POR THERMAL SENSORS : TO BE USED IN PRODUCTION

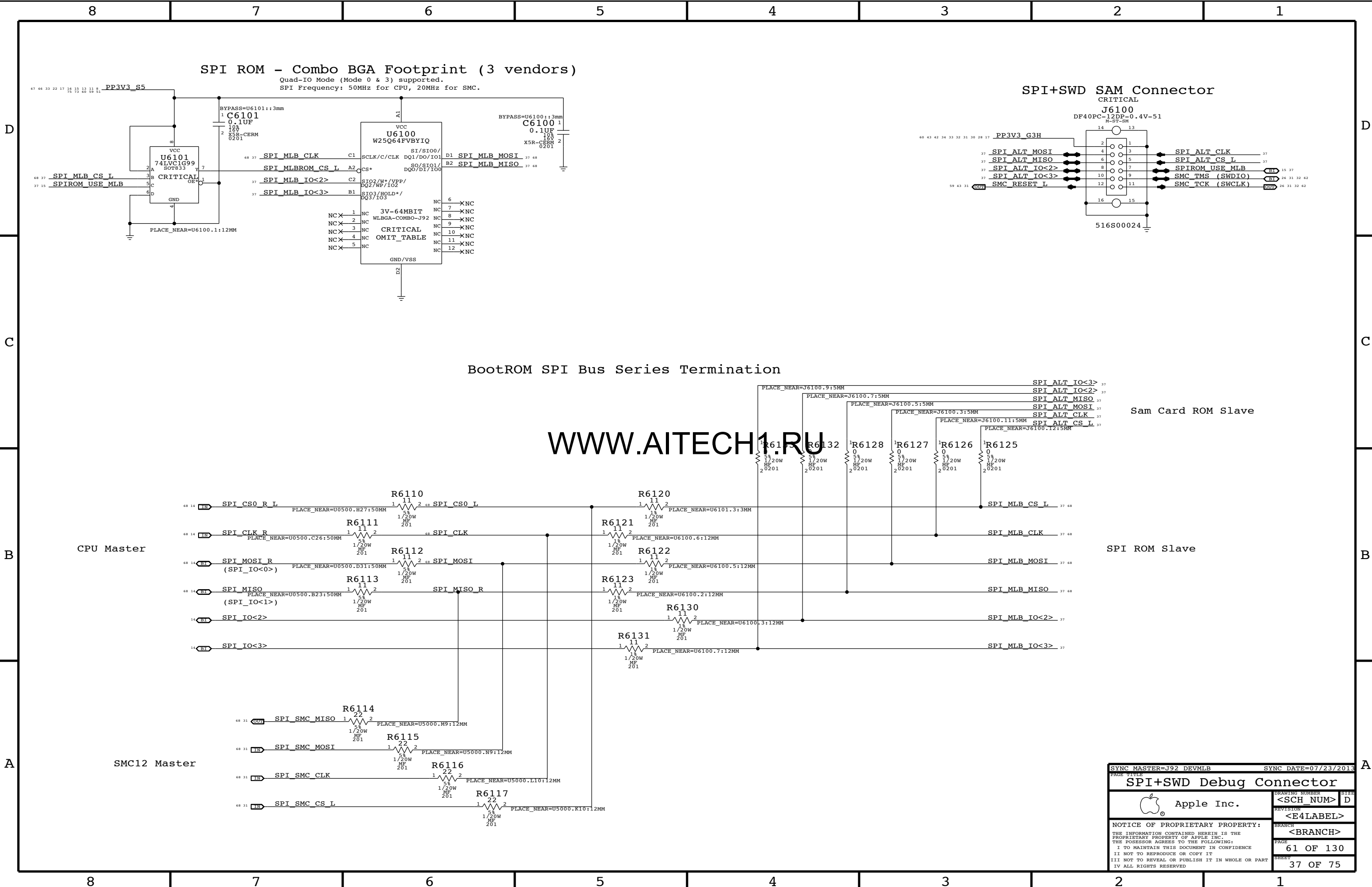
CPU Proximity, Inlet ,DDR and BMON THR Sensor



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NAND Temp Sensor





SPI ROM - Combo BGA Footprint (3 vendors)

Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

SPI+SWD SAM Connector

CRITICAL

J6100

DF40PC-12DP-0.4V-51
M-ST-SM

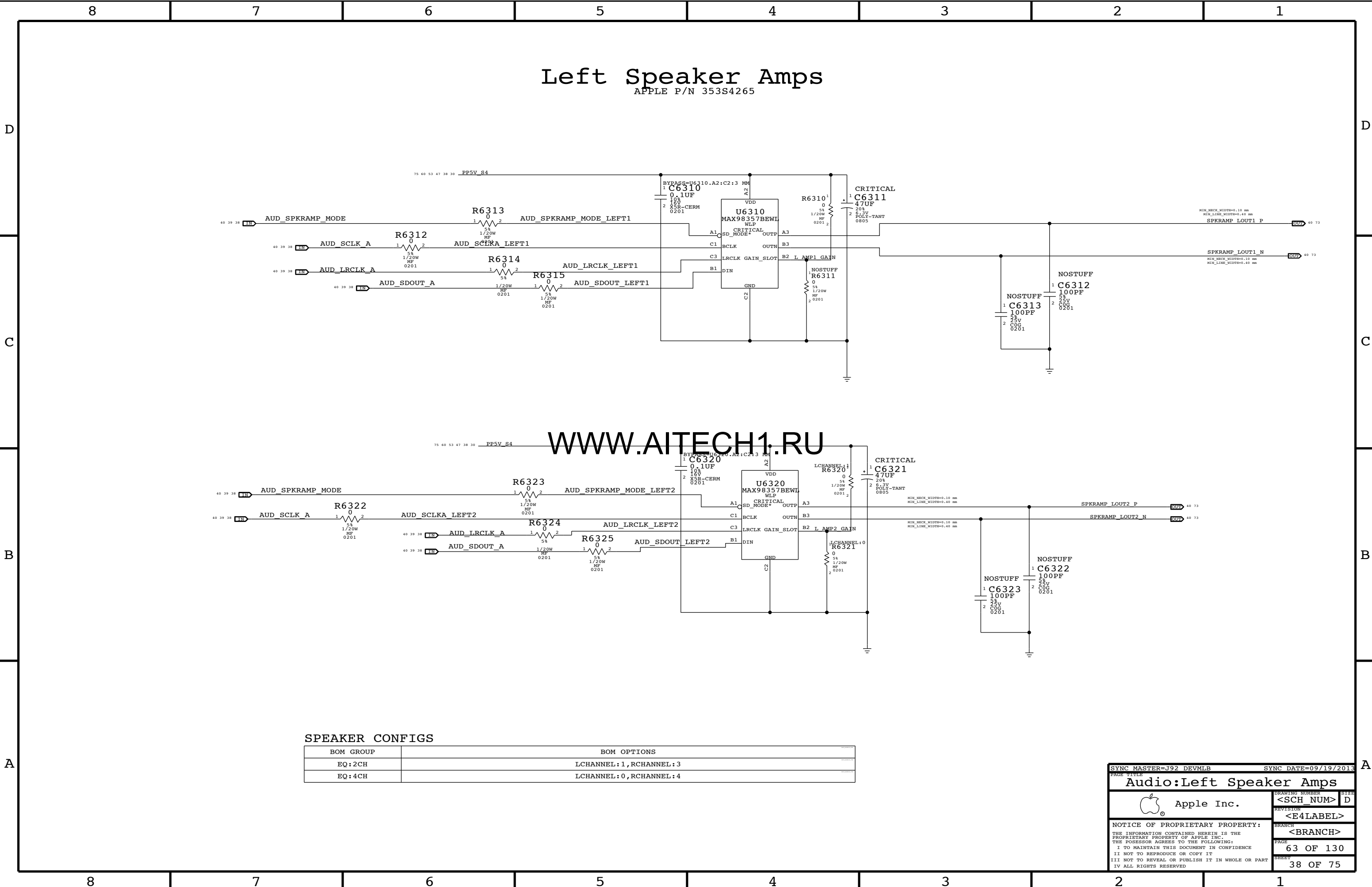
BootROM SPI Bus Series Termination

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Sam Card ROM Slave

SPI ROM Slave

PAGE TITLE		SYNC DATE=07/23/2013	
SYNC MASTER=J92 DEVMLB		SPI+SWD Debug Connector	
Apple Inc.		DRAWING NUMBER	SIZE
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		<BRANCH>	
		PAGE	61 OF 130
		SHEET	37 OF 75
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SPEAKER CONFIGS

BOM GROUP	BOM OPTIONS
EQ: 2CH	LCHANNEL: 1, RCHANNEL: 3
EQ: 4CH	LCHANNEL: 0, RCHANNEL: 4

SYNC MASTER=J92 DEVMLB

SYNC DATE=09/19/2013

Audio:Left Speaker Amps

Apple Inc.

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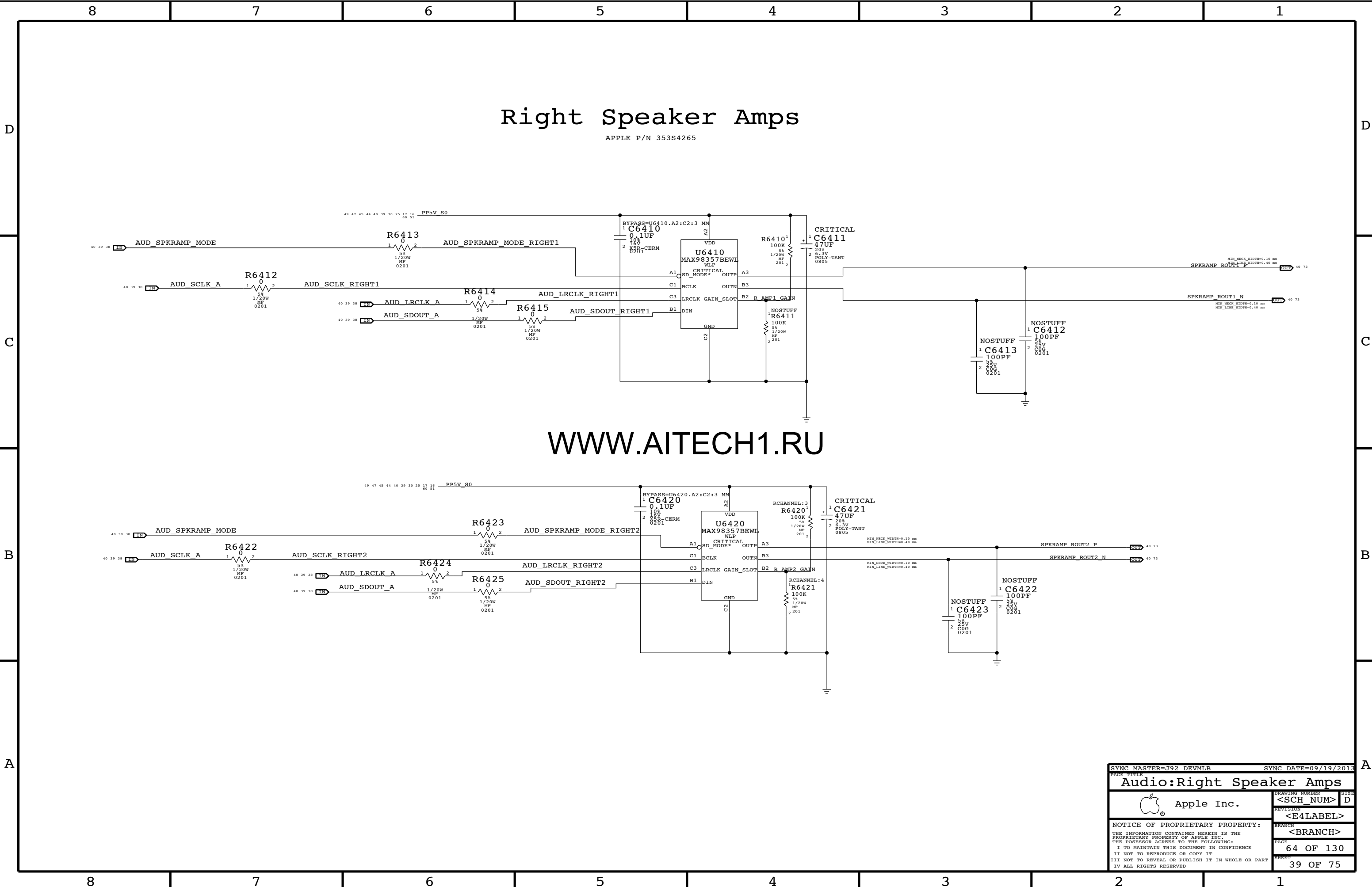
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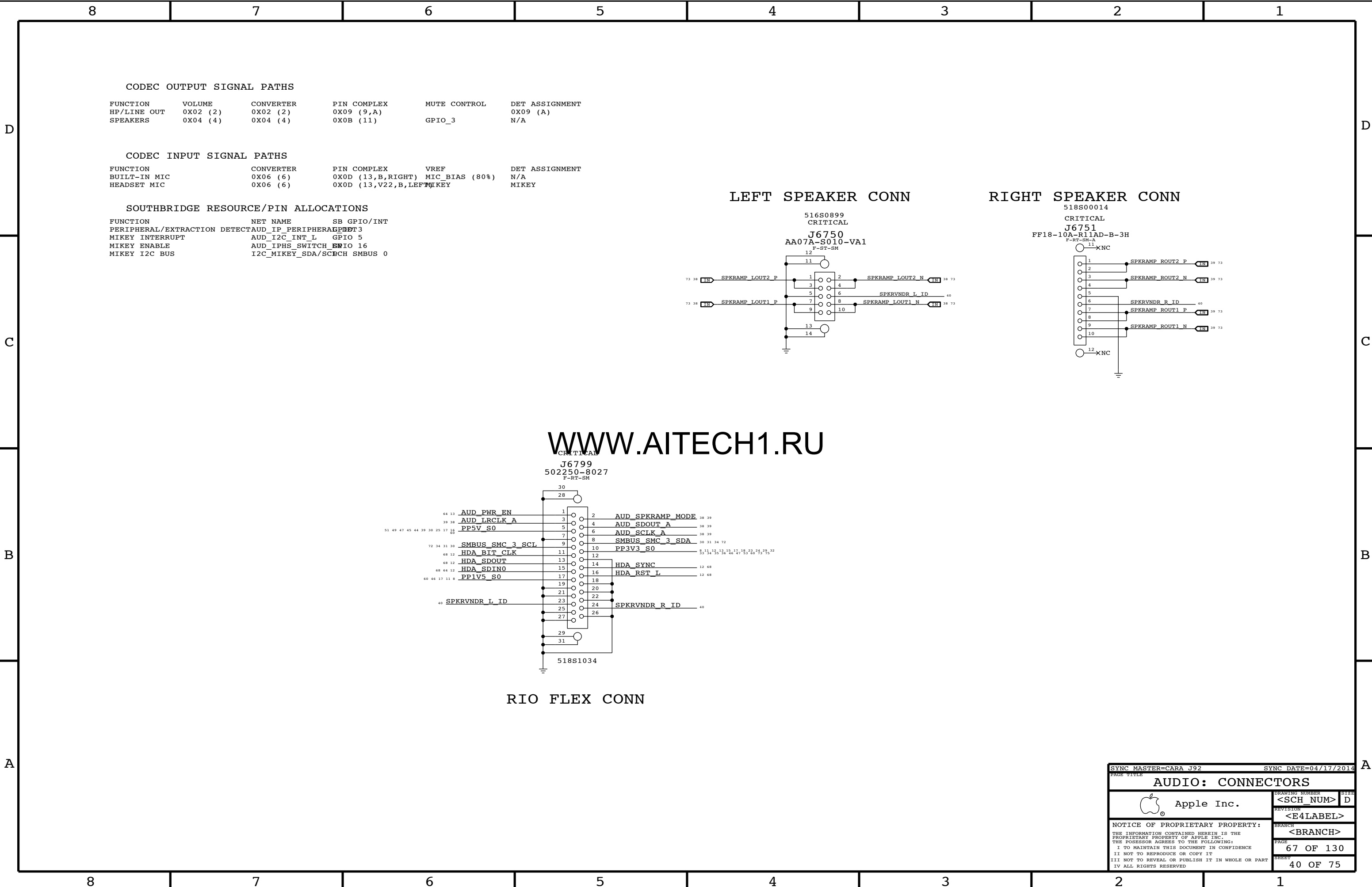
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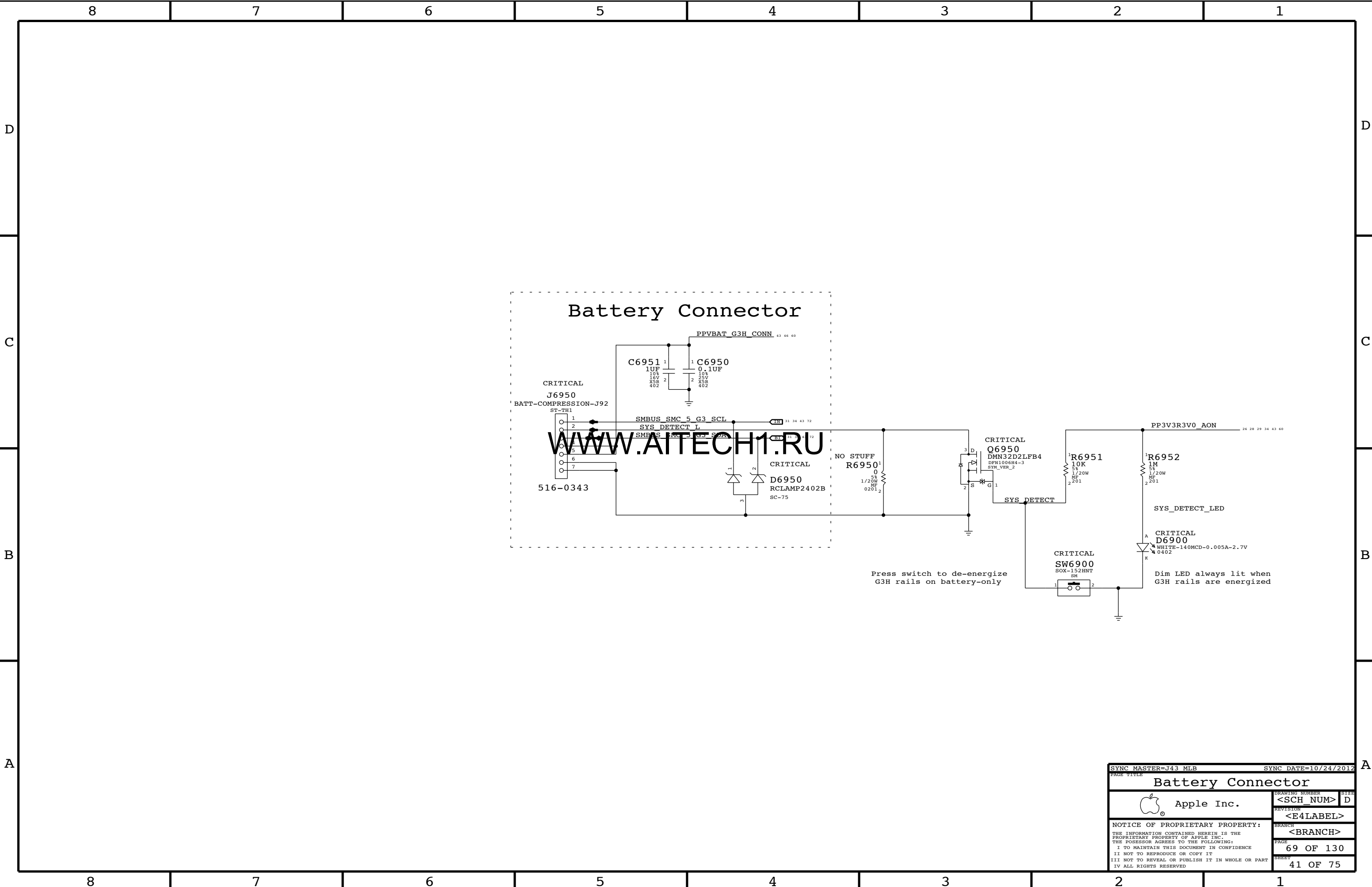
PAGE
63 OF 130


SHEET
38 OF 75

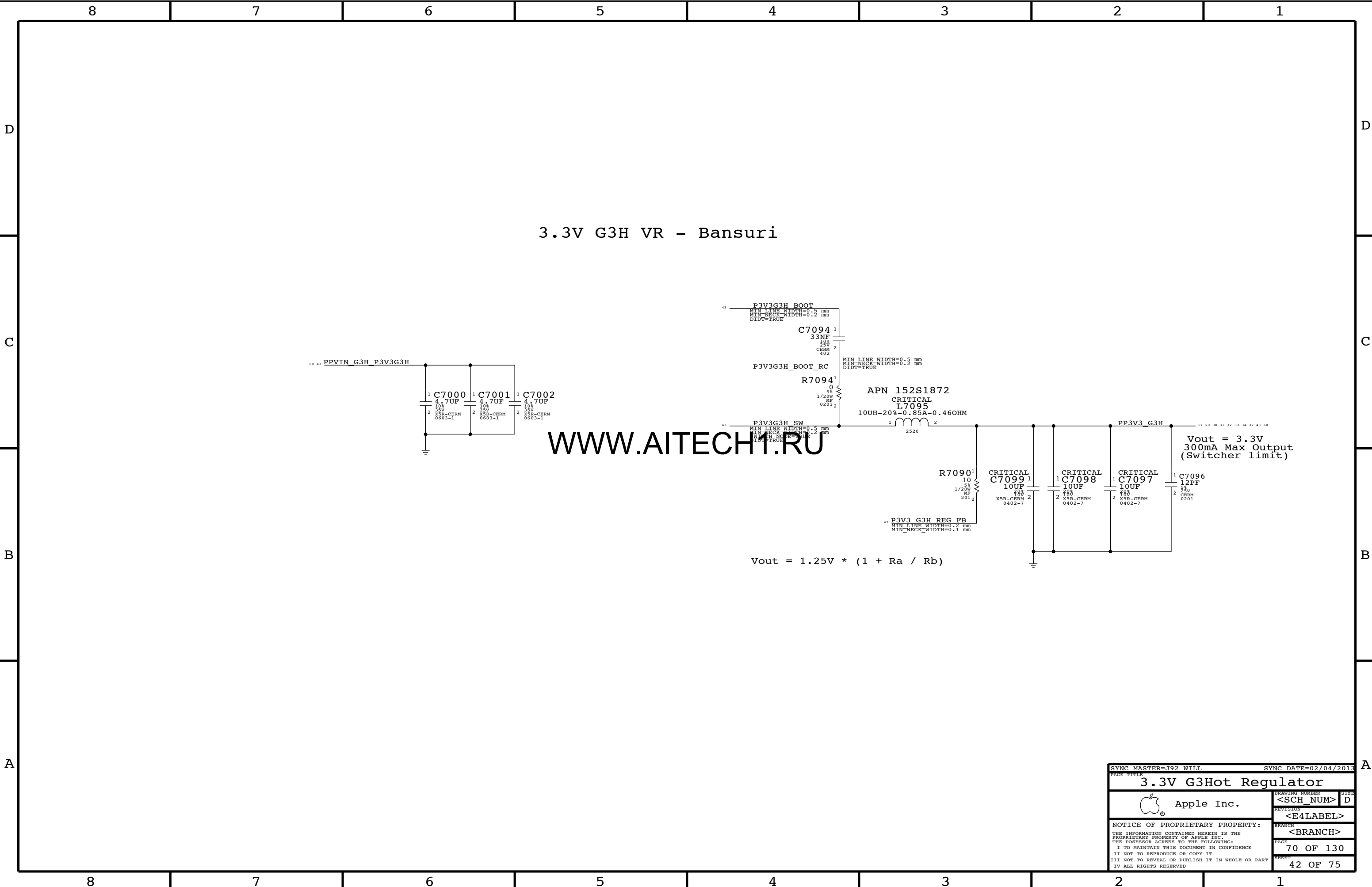




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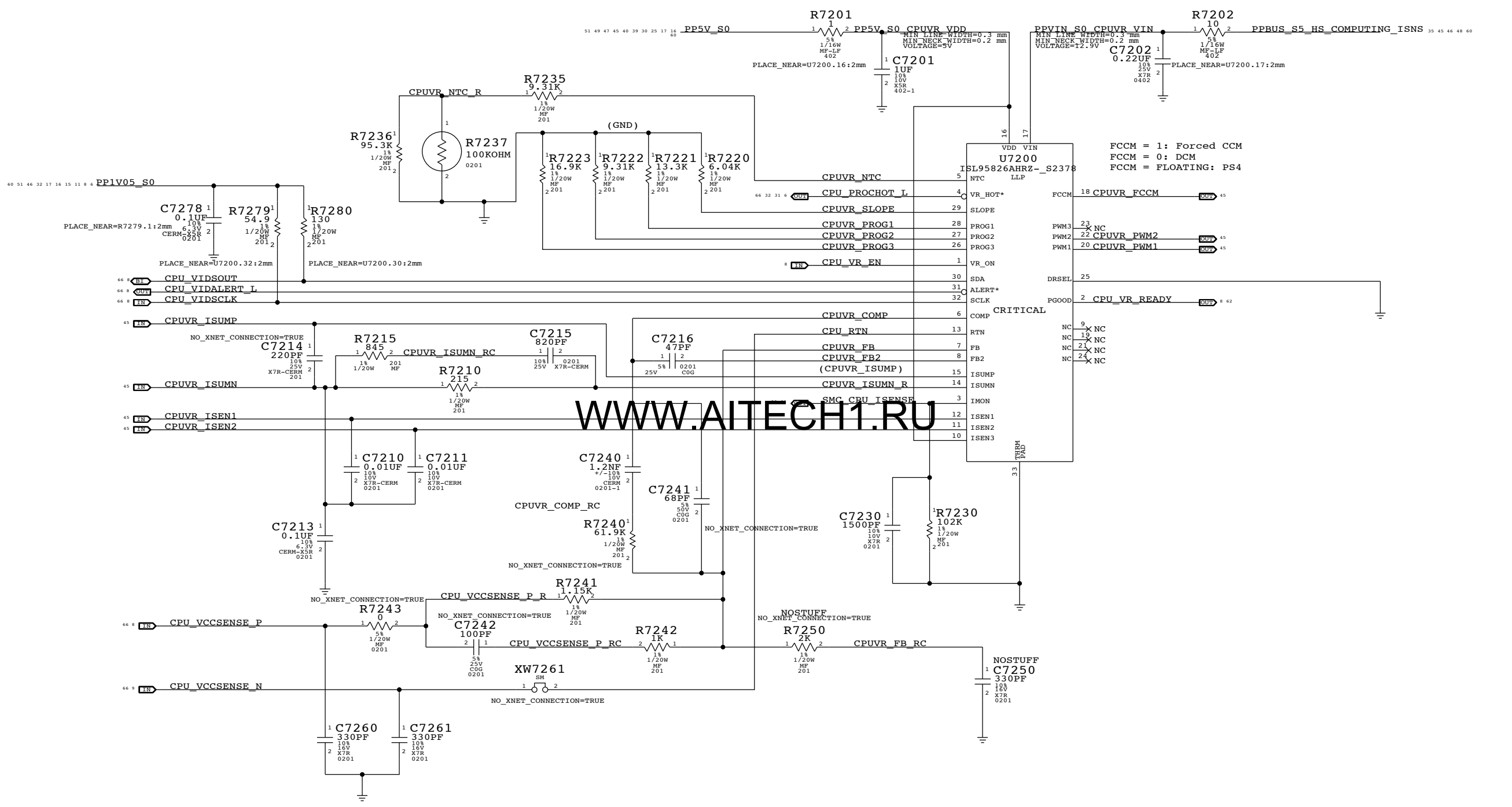
SYNC MASTER=J43 MLB		SYNC DATE=10/24/2012	
PAGE TITLE			
Battery Connector			
 Apple Inc.	DRAWING NUMBER		SIZE
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PAGE		69 OF 130	
SHEET		41 OF 75	

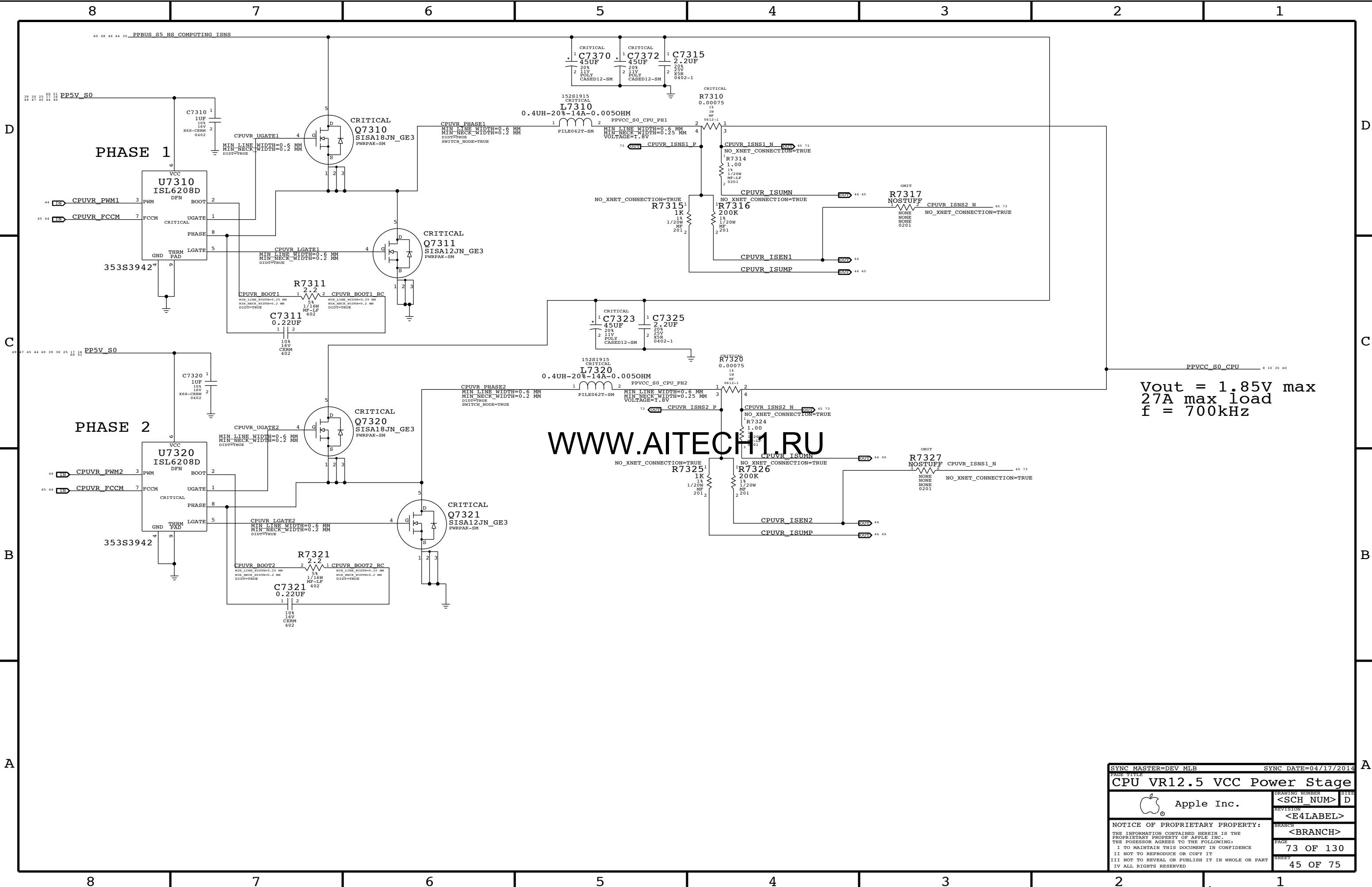



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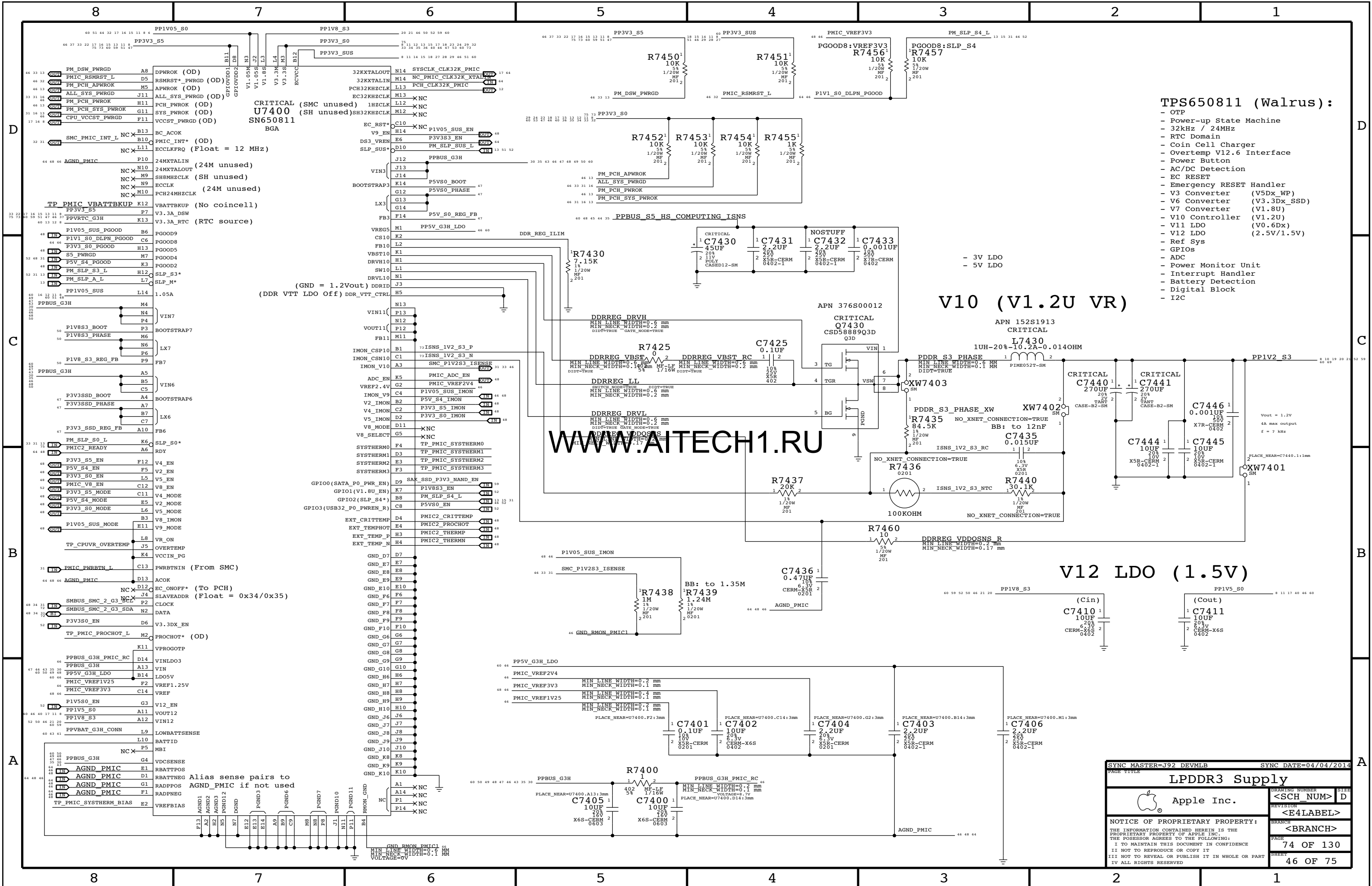
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00347	1	IC, ISL95530BIT11, CHGR PMU, HANSURI, WCP56	U7100	CRITICAL	

SYNC MASTER=J92 DEVMLB		SYNC DATE=04/04/2014	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.		DRAWING NUMBER <SCH NUM>	
		REVISION <E4LABEL>	
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SYNC MASTER=DEV MLB		SYNC DATE=04/17/2014		
PAGE TITLE				
CPU VR12.5 VCC Power Stage				
 Apple Inc.	DRAWING NUMBER		SIZE	
	<SCH_NUM>		D	
	REVISION		<E4LABEL>	
	BRANCH		<BRANCH>	
PAGE				
73 OF 130				
SHEET				
45 OF 75				



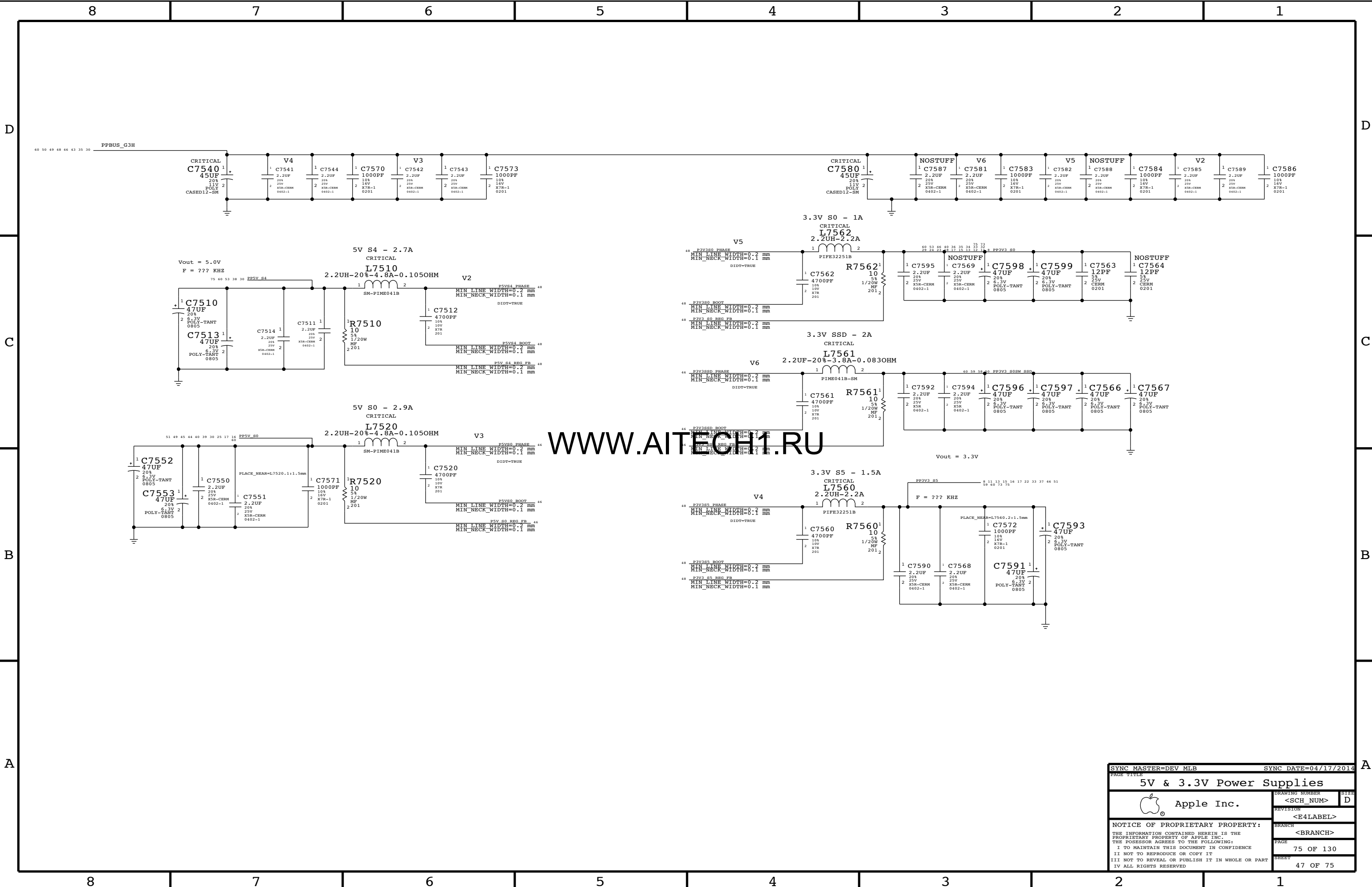
TPS650811 (Walrus):

- OTP
- Power-up State Machine
- 32kHz / 24MHz
- RTC Domain
- Coin Cell Charger
- Overtemp V12.6 Interface
- Power Button
- AC/DC Detection
- EC RESET
- Emergency RESET Handler
- V3 Converter (V5Dx_WP)
- V6 Converter (V3.3Dx_SSD)
- V7 Converter (V1.8U)
- V10 Controller (V1.2U)
- V11 LDO (V0.6Dx)
- V12 LDO (2.5V/1.5V)
- Ref Sys
- GPIOs
- ADC
- Power Monitor Unit
- Interrupt Handler
- Battery Detection
- Digital Block
- I2C


V10 (V1.2U VR)

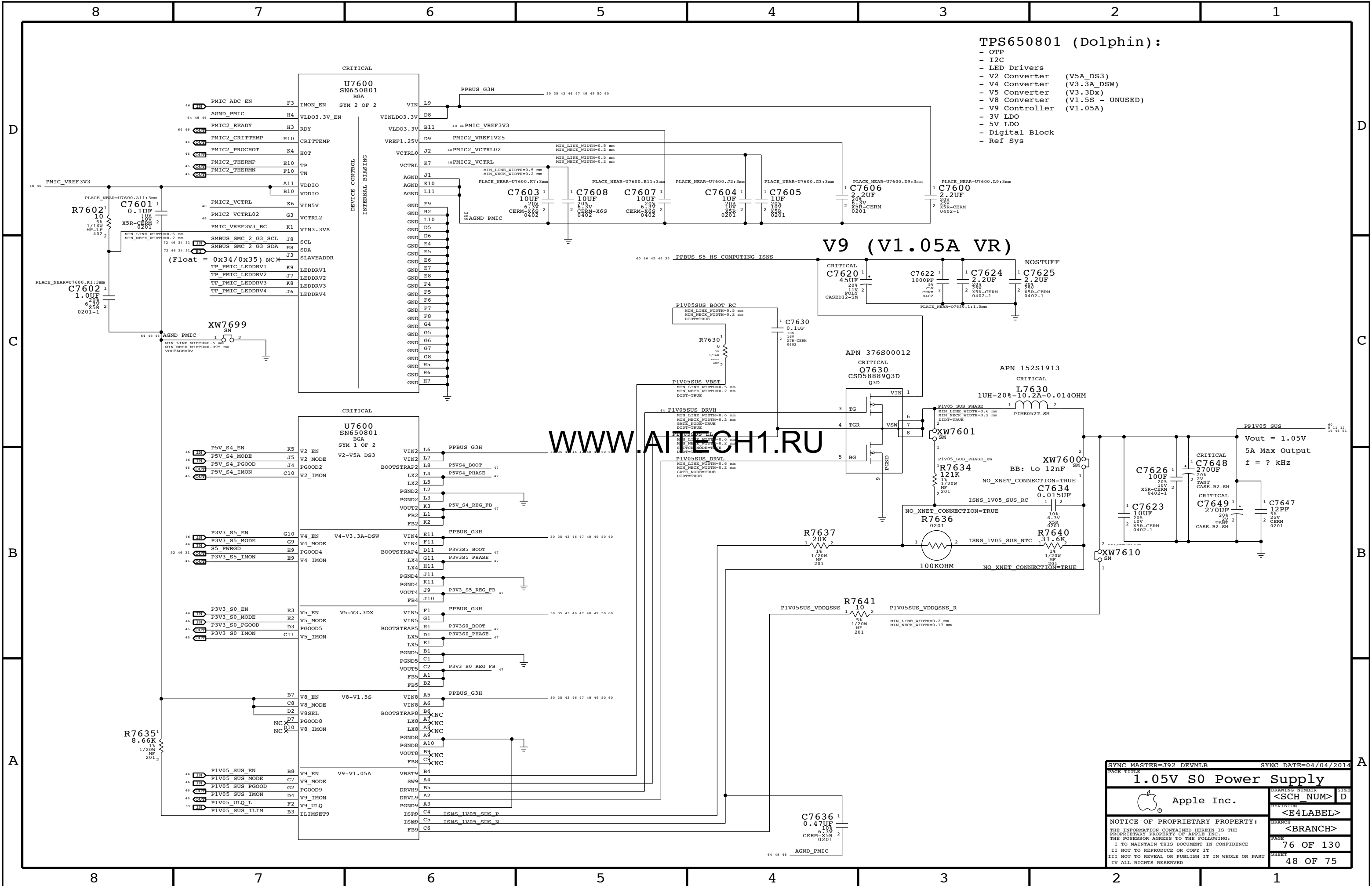
V12 LDO (1.5V)

SYNC MASTER=J92 DEVMLB		SYNC DATE=04/04/2014	
PAGE TITLE		LPDDR3 Supply	
Apple Inc.		REVISION	SIZE
		<SCH_NUM>	D
		REVISION	
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		PAGE	74 OF 130
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SYNC MASTER=DEV MLB		SYNC DATE=04/17/2014	
PAGE TITLE			
5V & 3.3V Power Supplies			
 Apple Inc.	DRAWING NUMBER	<SCH_NUM>	SIZE
	REVISION	<E4LABEL>	D
	BRANCH	<BRANCH>	
	PAGE	75 OF 130	
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TPS650801 (Dolphin):

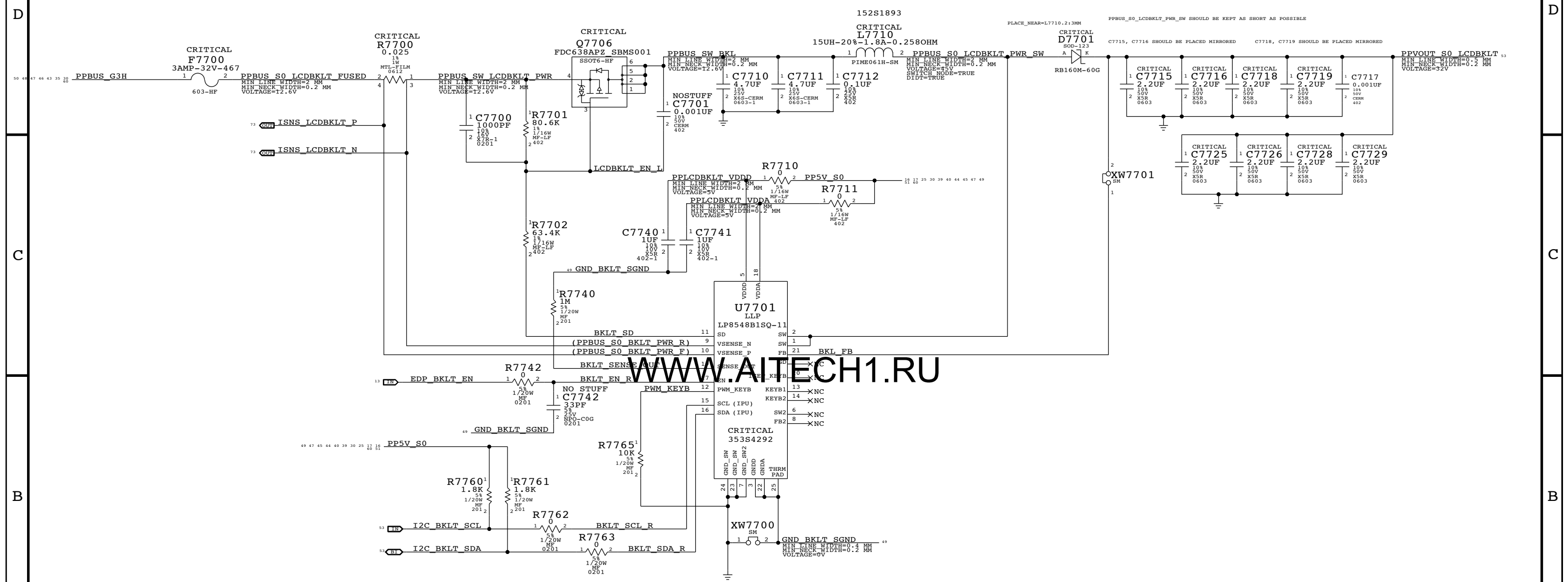
- OTP
- I2C
- LED Drivers
- V2 Converter (V5A_DS3)
- V4 Converter (V3.3A_DSW)
- V5 Converter (V3.3Dx)
- V8 Converter (V1.5S - UNUSED)
- V9 Controller (V1.05A)
- 3V LDO
- 5V LDO
- Digital Block
- Ref Sys


SYNC MASTER=J92 DEVMLB		SYNC DATE=04/04/2014	
PAGE TITLE		1.05V S0 Power Supply	
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		PAGE	76 OF 130
		SHEET	48 OF 75

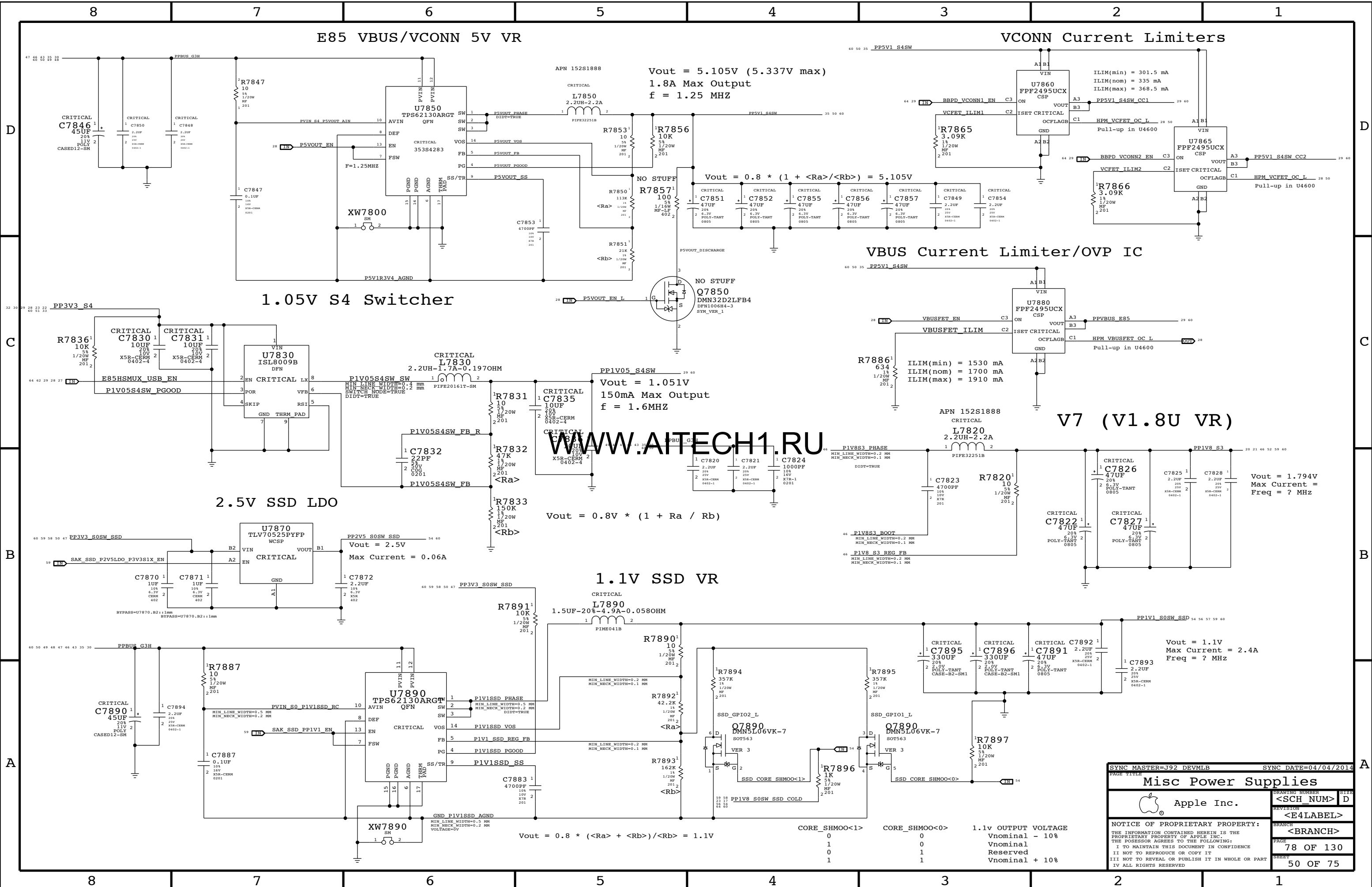
Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (6-8.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

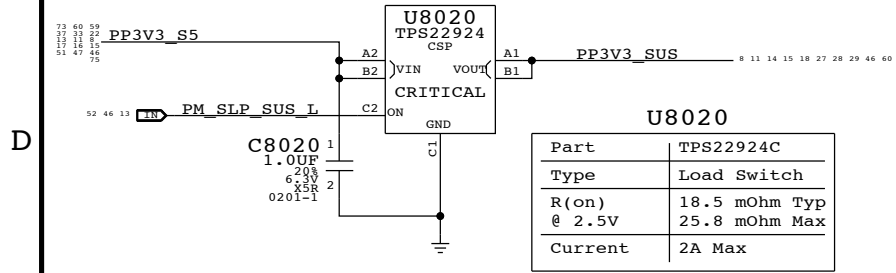


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LCD Backlight Driver			
 Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	77 OF 130
		SHEET	49 OF 75

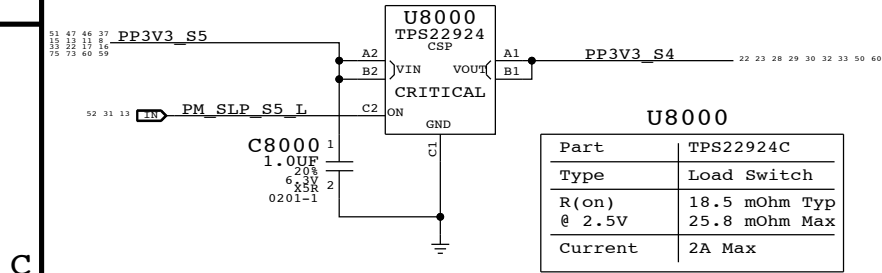


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Misc Power Supplies		<SCH_NUM> D	
Apple Inc.		REVISION	
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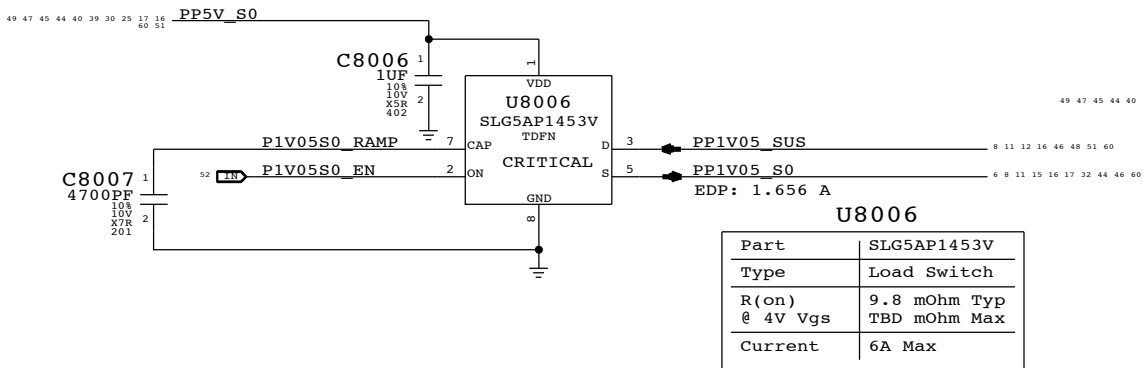
3.3V SUS Switch



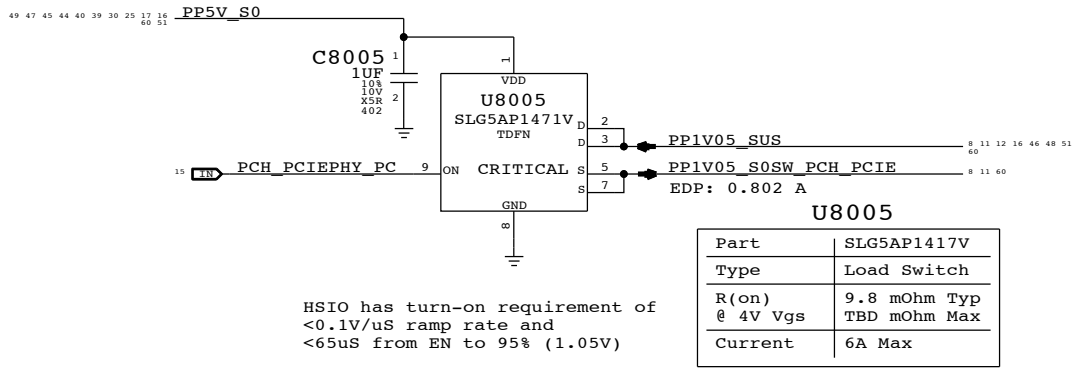
3.3V S4 Switch



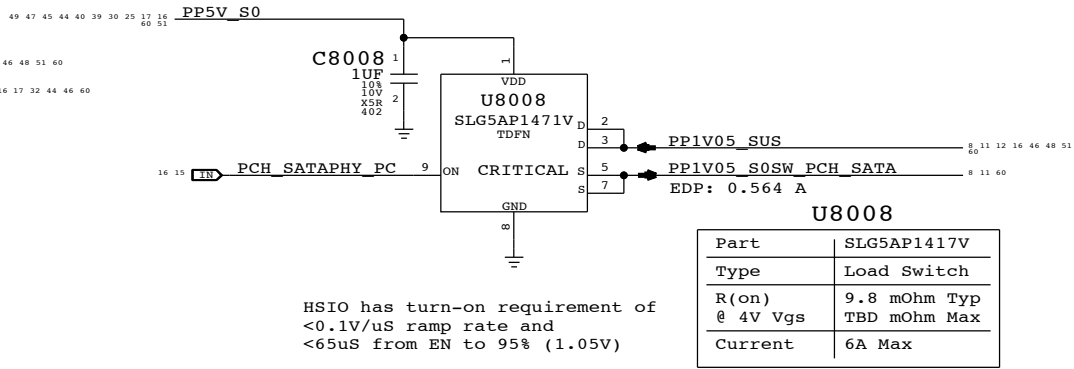
1.05V S0 Switch



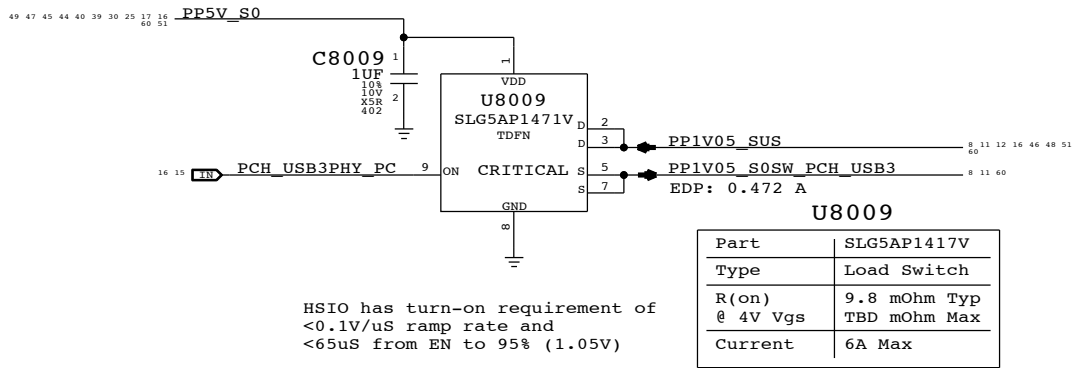
1.05V PCH PCIe Switch



1.05V PCH SATA Switch



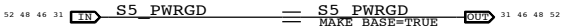
1.05V PCH USB3 Switch



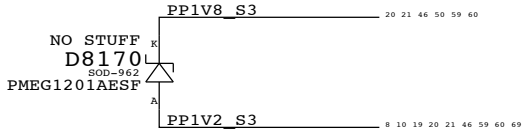
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Mobile System Power State Table							
State	SMC_ADAPTER_EN	SMC_PP0Z_ENABLE	SMC_S4_WAKEUP_EN	PM_SUS_EN	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S5)	0	1	1	1	1	1	0
Deep Sleep (S4AC)	1	1	1	0	0	0	0
Deep Sleep (S4)	0	1	1	0	0	0	0
Deep Sleep (S5AC)	1	1	0	0	0	0	0
Deep Sleep (S5)	0	1	0	0	0	0	0
Battery Off (G380SAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G380S)	1	0	0	0	0	0	0

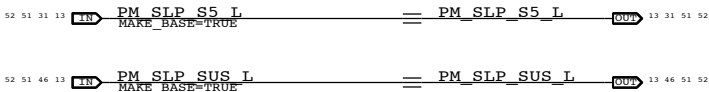
S5 Power Good



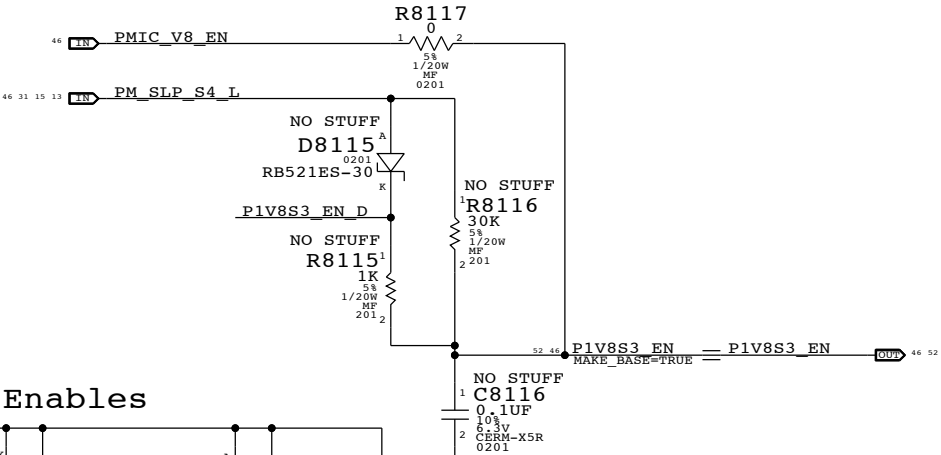
LPDDR power down sequencing support



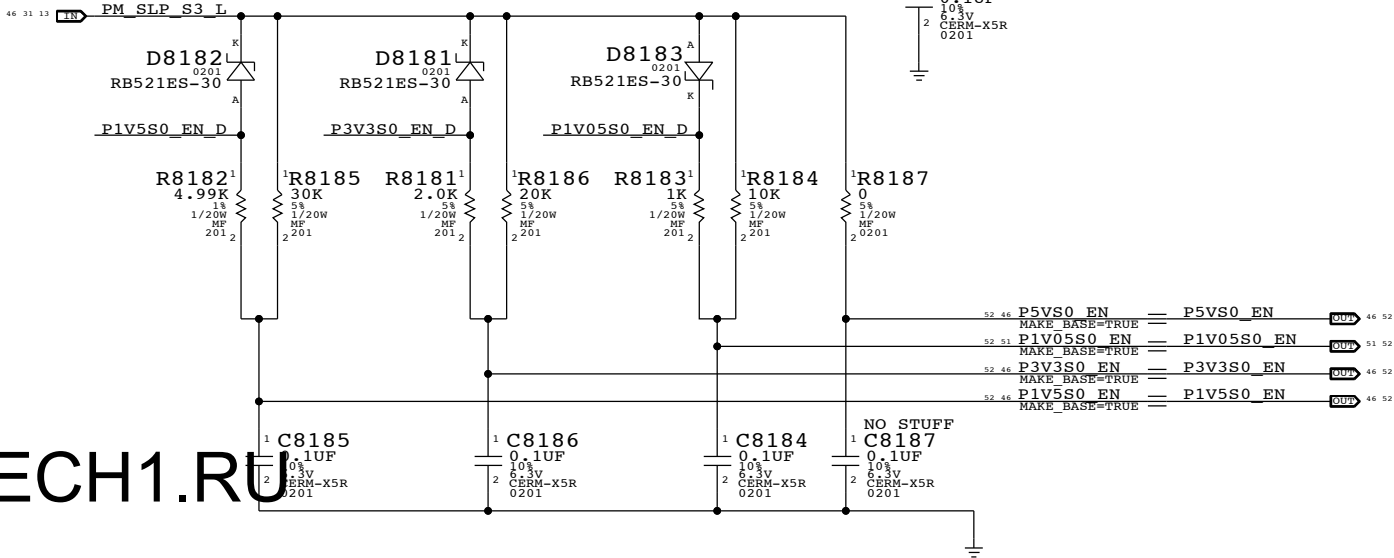
SUS & S4 Enables



S3 Enables

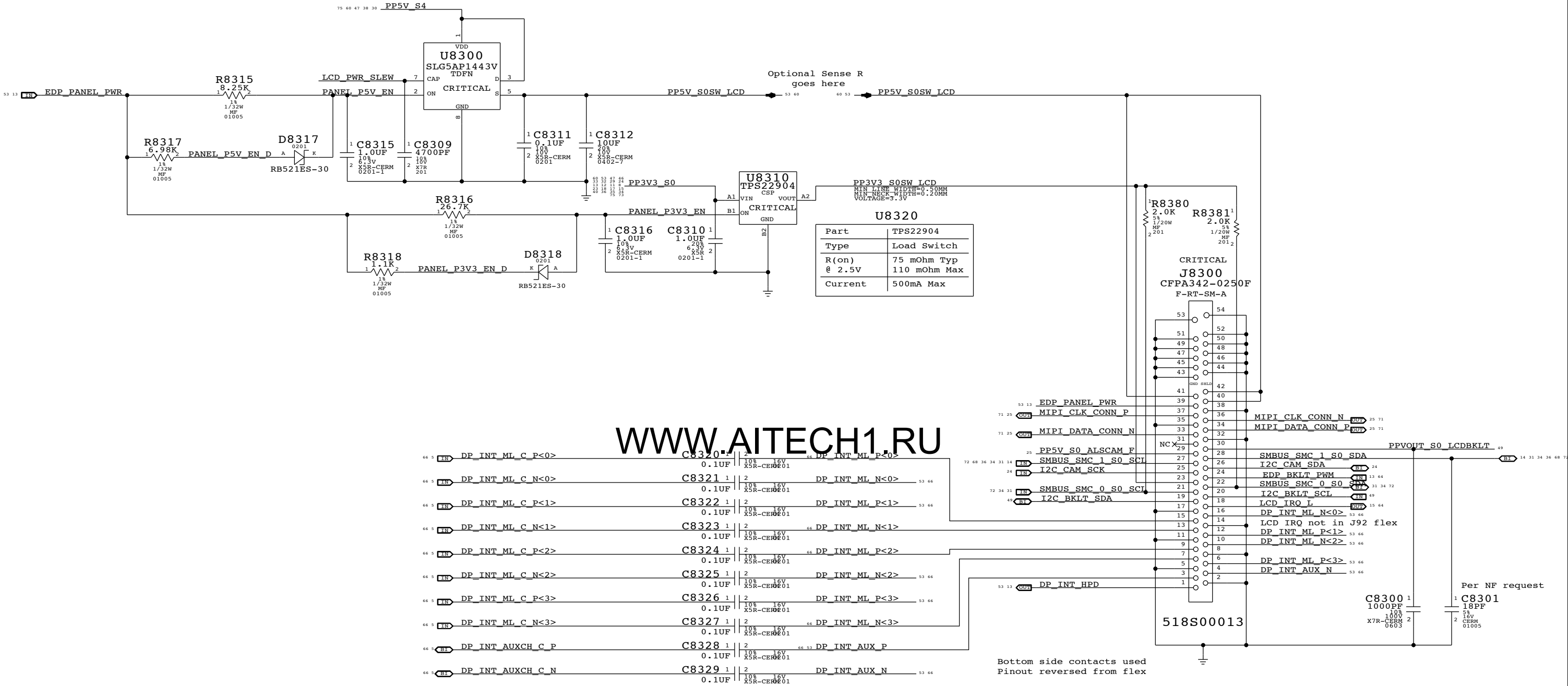


S0 Enables



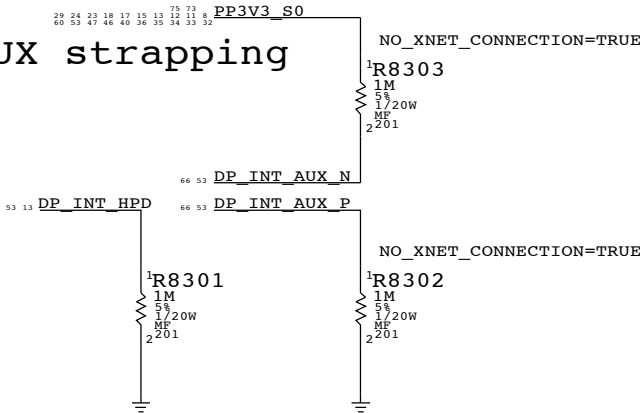
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LCD PANEL INTERFACE (eDP) + Camera (MIPI)

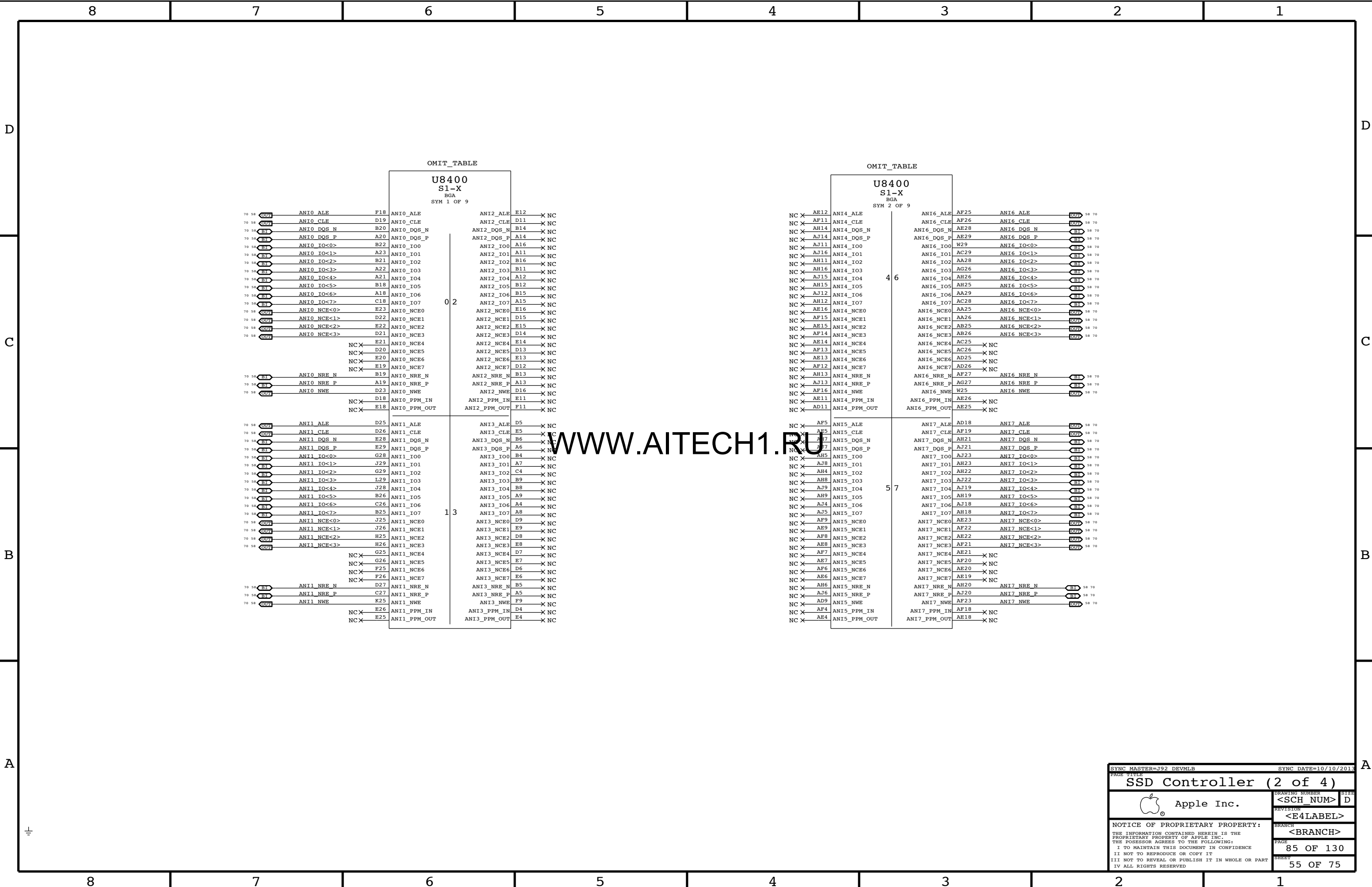


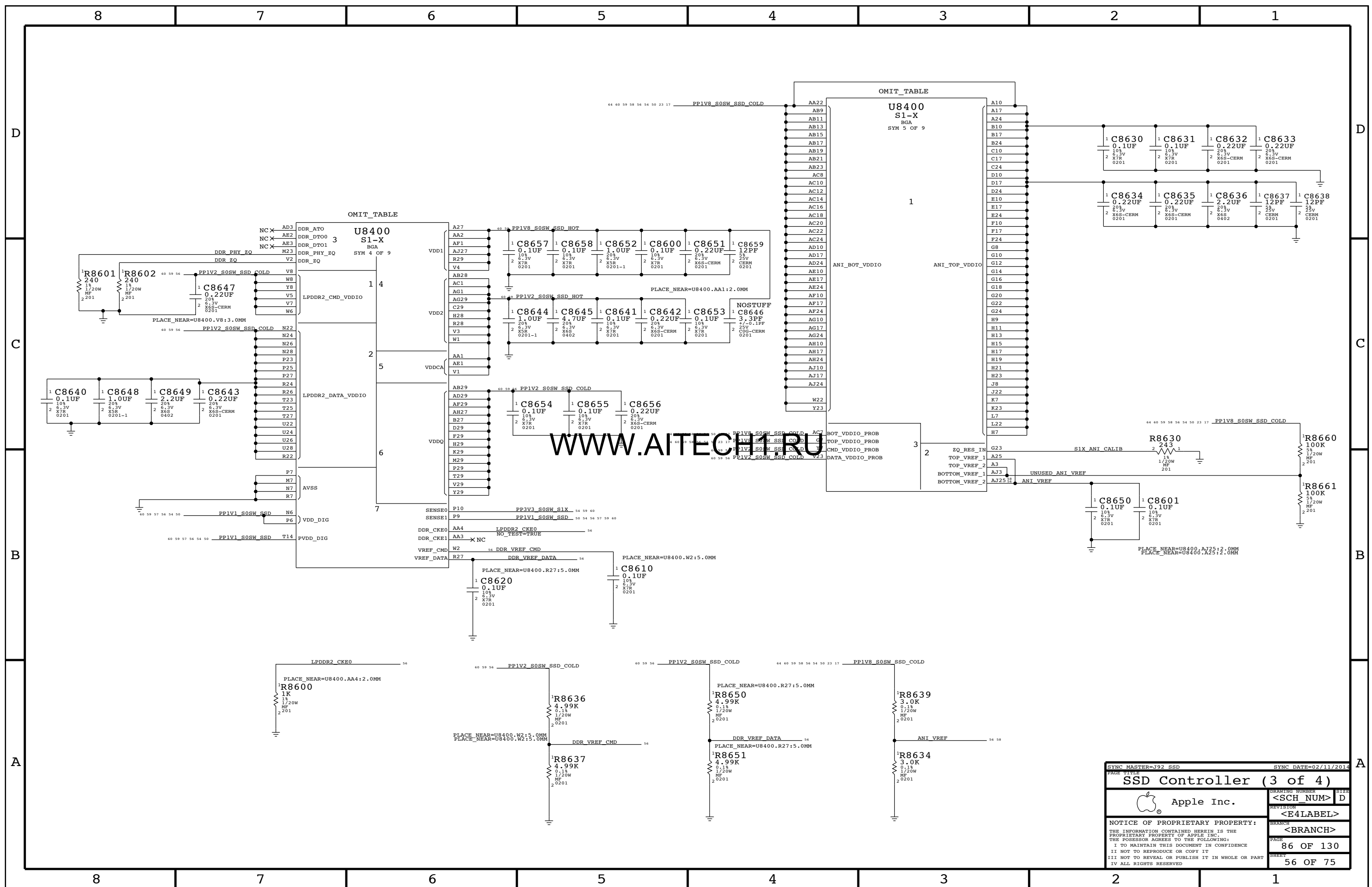
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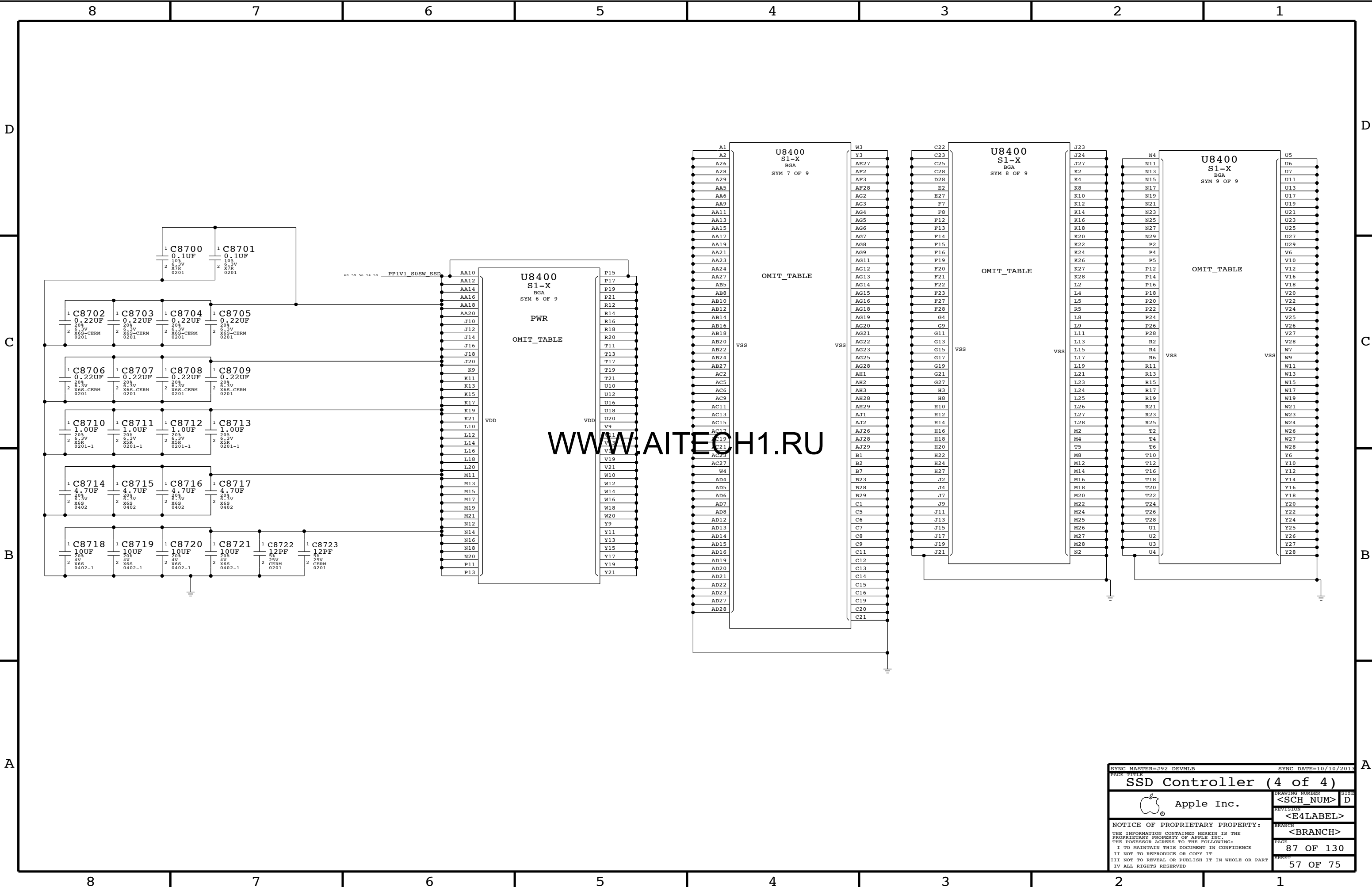
LCD Panel HPD & AUX strapping

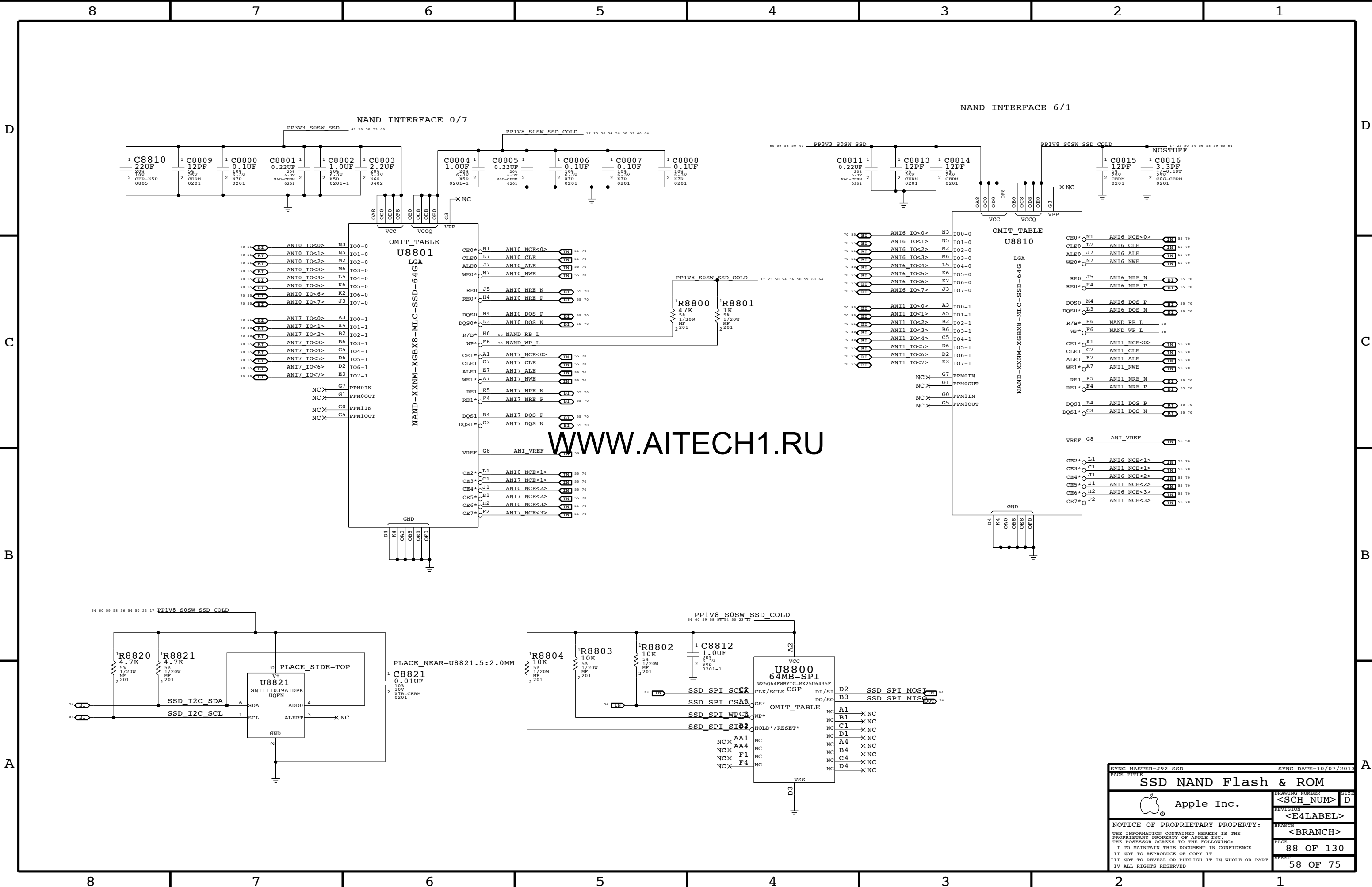


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eDP Display Connector			
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SYNC DATE=10/07/2013

SSD NAND Flash & ROM

 Apple Inc.

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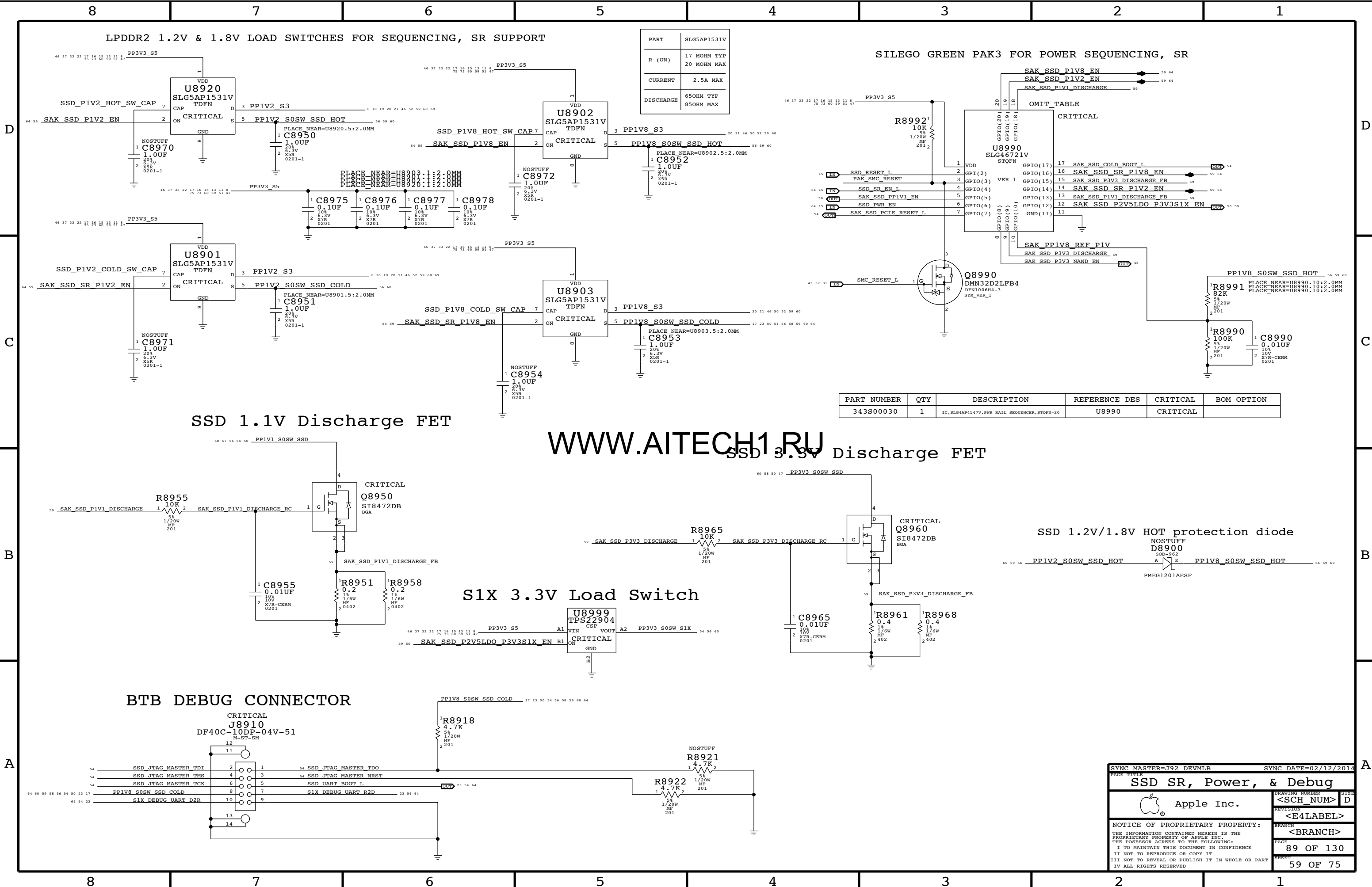
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PART	SLG5AP1531V
R (ON)	17 MOHM TYP 20 MOHM MAX
CURRENT	2.5A MAX
DISCHARGE	650HM TYP 850HM MAX

SILEGO GREEN PAK3 FOR POWER SEQUENCING, SR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00030	1	IC,SLG4AP4547V,PWR RAIL SEQUENCER,STQFN-20	U8990	CRITICAL	

SSD 1.1V Discharge FET


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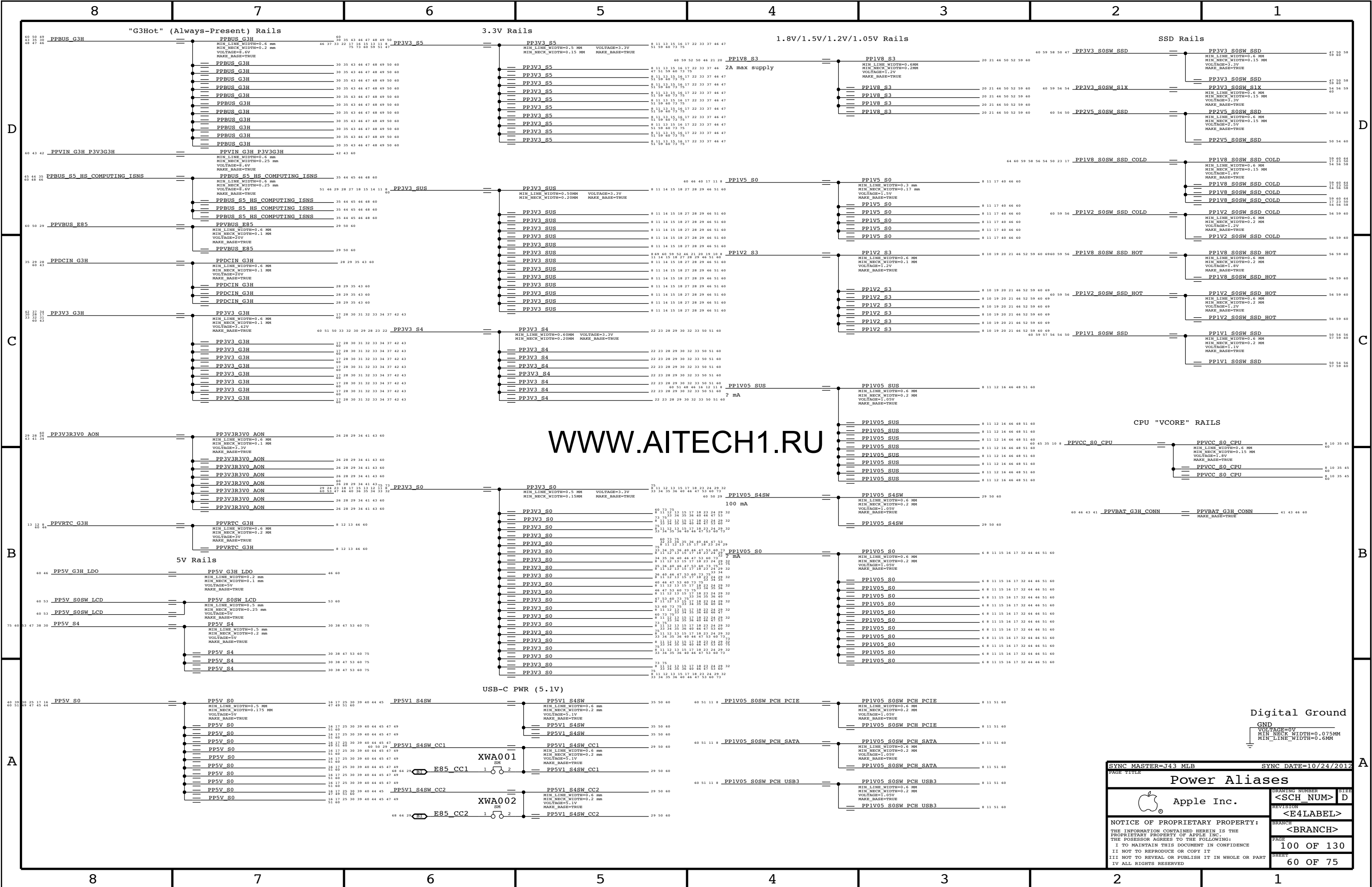
SSD 3.3V Discharge FET

S1X 3.3V Load Switch

SSD 1.2V/1.8V HOT protection diode

BTB DEBUG CONNECTOR

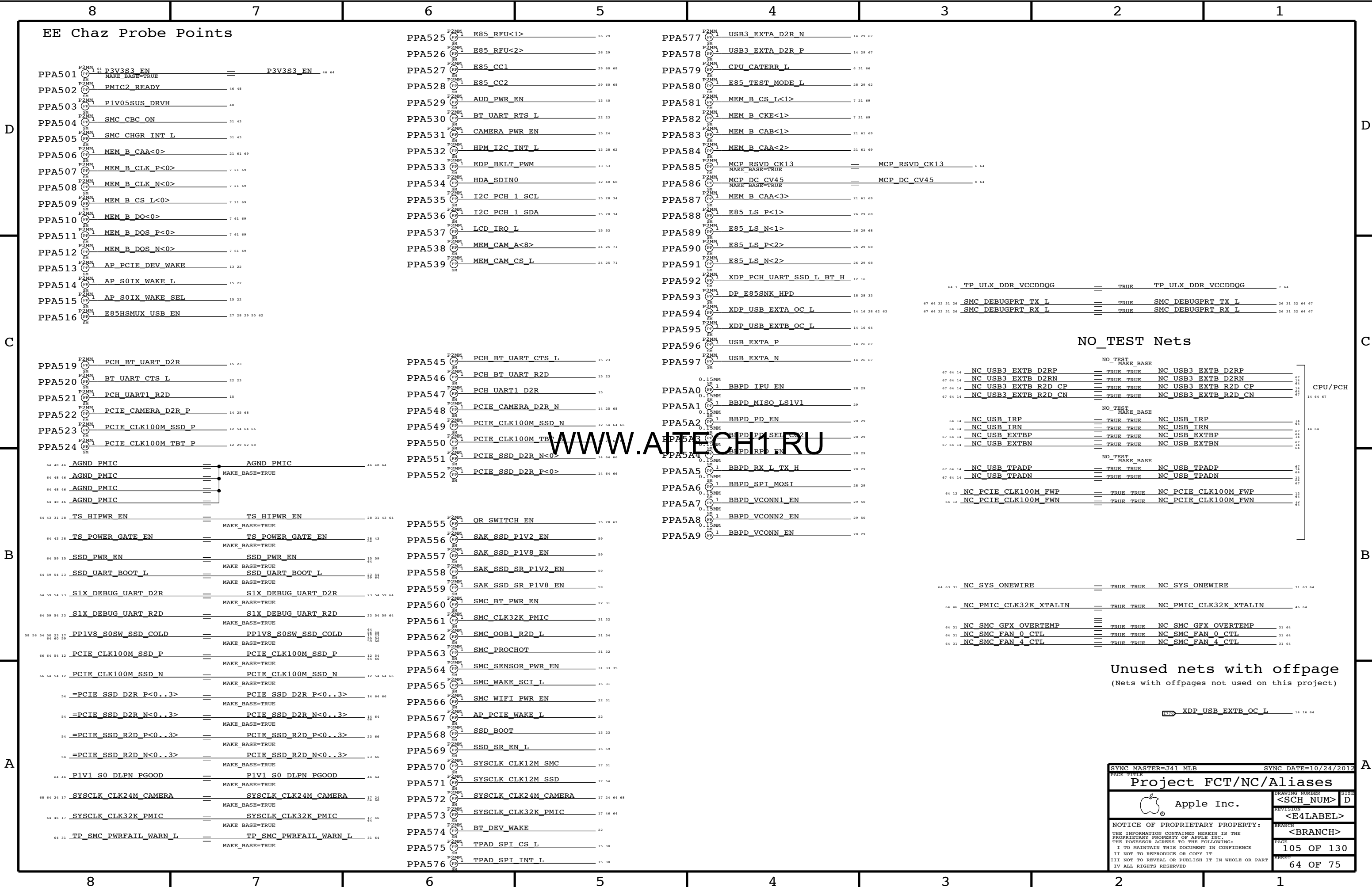
SYNC MASTER=J92 DEVMLB		SYNC DATE=02/12/2014	
PAGE TITLE			
SSD SR, Power, & Debug			
 Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
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		PAGE	89 OF 130
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	8	7	6	5	4	3	2	1
D	<pre> 64 62 28 15 OR_SWITCH_EN == MAKE_BASE OR_SWITCH_EN 15 28 62 64 TRUE 62 44 8 CPU_VR_READY == TRUE CPU_VR_READY 9 44 62 62 31 13 SMC_PCH_SUSWARN_L == TRUE SMC_PCH_SUSWARN_L 13 31 62 62 31 13 SMC_PCH_SUSACK_L == TRUE SMC_PCH_SUSACK_L 13 31 62 62 43 35 32 31 SMC_BC_ACOK == TRUE SMC_BC_ACOK 31 32 35 43 62 62 5 TP_ULX_SPARE1 == TRUE TP_ULX_SPARE1 5 62 62 5 TP_ULX_SSP_SPARE == TRUE TP_ULX_SSP_SPARE 5 62 68 62 12 TP_LPC_CLK24M_LPCPLUS_R == TRUE TP_LPC_CLK24M_LPCPLUS_R 12 62 68 64 62 28 13 HPM_I2C_INT_L == TRUE HPM_I2C_INT_L 13 28 62 64 64 62 28 13 HPM_I2C_INT_L == TRUE HPM_I2C_INT_L 13 28 62 64 63 62 28 16 14 XDP_USB_EXTN_OC_L == TRUE XDP_USB_EXTN_OC_L 14 16 28 62 63 64 62 37 32 31 26 SMC_TCK == TRUE SMC_TCK 26 31 32 37 62 62 37 32 31 26 SMC_TMS == TRUE SMC_TMS 26 31 32 37 62 62 28 TP_HPM_XTALOUT == TRUE TP_HPM_XTALOUT 28 62 GND == TRUE GND 68 64 62 29 12 PCIE_CLK100M_TBT_P == TRUE PCIE_CLK100M_TBT_P 12 29 62 64 68 68 64 62 29 12 PCIE_CLK100M_TBT_N == TRUE PCIE_CLK100M_TBT_N 12 29 62 64 68 29 =PCIE_E85_D2R_P == TRUE PCIE_TBT_D2R_P<0> 14 68 29 =PCIE_E85_D2R_N == TRUE PCIE_TBT_D2R_N<0> 14 68 29 =PCIE_E85_R2D_P == TRUE PCIE_TBT_R2D_C_P<0> 14 68 29 =PCIE_E85_R2D_N == TRUE PCIE_TBT_R2D_C_N<0> 14 68 62 29 12 TBT_CLKREQ_L == TRUE TBT_CLKREQ_L 12 29 62 62 29 15 PCH_TBT_PCIE_RESET_L == TRUE PCH_TBT_PCIE_RESET_L 15 29 62 64 62 29 28 E85_TEST_MODE_L == TRUE E85_TEST_MODE_L 28 29 62 64 64 62 50 29 28 27 <IN> E85HSMUX_USB_EN == E85HSMUX_USB_EN <OUT> 27 28 29 50 62 64 MAKE_BASE=TRUE </pre>							
C								
B								
A	WWW.AITECH1.RU							
	8	7	6	5	4	3	2	1
								<div> <div> <div> <div> <div>SYNC MASTER=J92 DEVMLB</div> <div>SYNC DATE=07/08/2014</div> </div> <div> <div>PAGE TITLE</div> <div>J92 Signal Aliases</div> </div> <div> <div> Apple Inc. </div> <div> <div>NOTICE OF PROPRIETARY PROPERTY:</div> <div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.</div> <div>THE POSSESSOR AGREES TO THE FOLLOWING:</div> <div>I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE</div> <div>II NOT TO REPRODUCE OR COPY IT</div> <div>III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART</div> <div>IV ALL RIGHTS RESERVED</div> </div> </div> <div> <div>DRAWING NUMBER</div> <div><SCH_NUM></div> <div>REVISION</div> <div><E4LABEL></div> <div>BRANCH</div> <div><BRANCH></div> <div>PAGE</div> <div>103 OF 130</div> <div>SHEET</div> <div>62 OF 75</div> </div> </div> </div> </div>





CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

Note: CPU_8MIL and CPU_ITP can be converted back to TABLE_SPACING_RULE once rdar://10308147 is resolved

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE SET
CPU_8MIL	*	*	CPU_8MIL_2AN

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_8MIL_2ANY	*	8 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CPU_ITP	*	*	CPU_ITP_2ANY

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ITP_2ANY	*	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CPU_COMP	CPU_COMP	*	CPU_COMP_2SE
CPU_COMP	*	*	CPU_COMP_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	*	=4x_DIELECTRIC	?
CPU_COMP_2OTHER	*	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SE
CPU_VCCSENSE	*	*	CPU_VCCSENSE_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIE Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SELECTOR
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SEMI
CLK_PCIE	*	*	CLK_PCIE_20TH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CLK_PCIE_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SH
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHER
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHER
PCIE_CPU_TX	*_CPU_RX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERH
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERH
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERH
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERH
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX20THERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX20THERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_20THERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_20THER	TOP,BOTTOM	=5x_DIELECTRIC	?

PCH PCIE Spacing			
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SH
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHER
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHER
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_20THERH
PCIE_PCH_RX	*_TX	*	PCIE_20THERH
PCIE_PCH_TX	*_RX	*	PCIE_20THERH
PCIE_PCH_RX	*_RX	*	PCIE_20THERH
PCIE_PCH_TX	*	*	PCIE_20THER
PCIE_PCH_RX	*	*	PCIE_20THER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX20THERTX	*	=4x_DIELECTRIC	?
PCIE_RX20THERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_20THERHS	*	=4x_DIELECTRIC	?
PCIE_20THER	*	=3x_DIELECTRIC	?

Note: DisplayPort tables are on Page 113

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.


CPU Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL	NET_TYPE	SPACING	
	CPU_PECI	CPU_45S	CPU_COMP	CPU_PECI	6 32
	PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	
	PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	
		CPU_45S	CPU_ITP	XDP DBRESET_L	16 17
		CPU_45S	CPU_TTP	XDP_CPU_PRDY_L	6 16
		CPU_45S	CPU_TTP	XDP_CPU_PREQ_L	6 16
		CPU_27F4S	CPU_COMP	EDP_COMP	
		CPU_27F4S	CPU_COMP	CPU_PEG_COMP	
	CPU_SM_RCOMP	CPU_27F4S	CPU_COMP	CPU_SM_RCOMP<0>	6
	CPU_SM_RCOMP	CPU_27F4S	CPU_COMP	CPU_SM_RCOMP<1>	6
	CPU_SM_RCOMP	CPU_27F4S	CPU_COMP	CPU_SM_RCOMP<2>	6
	CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<2..0>	6 16
	CPU_CFG3	CPU_45S	CPU_ITP	CPU_CFG<3>	6 16
	CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..4>	6 16
	CPU_CATERR_I	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 31 64
		CPU_45S	CPU_AGTL	CPU_VCCIO_SEL	
	CPU_PROCHOT_I	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 31 32 64
	CPU_EWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6
	PM_THRMTRIP_I	CPU_45S	CPU_BMTL	PM_THRMTRIP_L	15 31 32
	DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M CPU P	
	DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M CPU N	
	DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP	
	DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITXPDP_CLK100M_P	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITXPDP_CLK100M_N	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P	
	ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N	
	XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 16
	XDP_TDO	CPU_45S	CPU_TTP	XDP_CPU_TDO	6 16
	XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 16
	XDP_TCK	CPU_45S	CPU_TTP	XDP_CPU_TCK	6 16
	XDP_TRST_I	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 12 16
	XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<1..0>	6 16
		CPU_45S	CPU_ITP	XDP_BPM_L<7..2>	6 16
		CPU_45S	CPU_TTP	XDP_OBSDATA_B<3..0>	
	(FSB_CPURST_L)	CPU_45S	CPU_ITP	XDP_CPURST_L	16
	CPU_VCCSENSE	SENSE_I701_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P	8 44
	CPU_VCCSENSE	SENSE_I701_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N	9 44
	CPU_VCCIOSENSE	SENSE_I701_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P	
	CPU_VCCIOSENSE	SENSE_I701_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N	
	CPU_AXG_SENSE	SENSE_I701_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P	
	CPU_AXG_SENSE	SENSE_I701_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N	
	CPU_VDDO_SENSE	CPU_27F4S	CPU_VCCSENSE	CPU_VDDO_SENSE_P	
	CPU_VDDO_SENSE	CPU_27F4S	CPU_VCCSENSE	CPU_VDDO_SENSE_N	
	CPU_VALSENSE	CPU_27F4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	
	CPU_VALSENSE	CPU_27F4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	
	CPU_VALSENSE	CPU_27F4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	
	CPU_VALSENSE	CPU_27F4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	
	CPU_SVIDALERT_I	CPU_45S	CPU_COMP	CPU VIDALERT_L	8 44
	CPU_SVIDSCLK	CPU_45S	CPU_COMP	CPU VIDSCLK	8 44
	CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU VIDSOUT	8 44
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D_C P<3..0>	14 23
	PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D_C N<3..0>	14 23
		PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D_P<3..0>	23 64
		PCIE_80D	PCIE_CPU_TX	PCIE SSD R2D_N<3..0>	23 64
		PCIE_80D	PCIE_CPU_RX	PCIE SSD D2R_C P<3..0>	54
		PCIE_80D	PCIE_CPU_RX	PCIE SSD D2R_C N<3..0>	54
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE SSD D2R_P<3..0>	14 64
	PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE SSD D2R_N<3..0>	14 64
	PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_SSD_P	12 54 64
	PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE CLK100M_SSD_N	12 54 64

Note: 80ohm constraints are actually 85ohm

PCIe SSD

DP

SYNCH MASTER=J92 DEVMLB		SYNCH DATE=07/08/2014	
PAGE TITLE			
CPU Constraints			
 Apple Inc.		DRAWING NUMBER <SCH NUM>	
		SIZE <E4LABEL>	
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ICOMP	*	=4x_DIELECTRIC	?

E85 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
E85_HS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
E85_LS_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
E85_HS	*	=6x_DIELECTRIC	?
E85_LS	*	=4x_DIELECTRIC	?
E85_CC	*	=4x_DIELECTRIC	?

SOURCE: 471984_Chief_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

UART Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
UART_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
UART	*	=2x_DIELECTRIC	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX	USB3_PCH_TX	*	USB3_TX2TX	USB3_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	USB3_PCH_RX	*	USB3_RX2RX	USB3_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_TX	*	USB3_TX2OTHERTX	USB3_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_RX	*	USB3_RX2OTHERRX	USB3_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_PCH_RX	*	USB3_TX2RX	USB3_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_RX	*_PCH_TX	*	USB3_RX2TX	USB3_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
USB3_PCH_TX	*_TX	*	USB3_2OTHERHS	USB3_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_RX	*_TX	*	USB3_2OTHERHS	USB3_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_TX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_RX	*_RX	*	USB3_2OTHERHS				
USB3_PCH_TX	*	*	USB3_2OTHER				
USB3_PCH_RX	*	*	USB3_2OTHER				

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET		NET TYPE		
		PHYSICAL	SPACING	
		SPT_45S	SPT	TPAD SPI MOSI 15 30
		SPT_45S	SPT	TPAD SPI MISO 15 30
		SPT_45S	SPT	TPAD SPI CLK 15 30
	USB_BT	USB_80D	USB	USB_BT_P 14 22
	USB_BT	USB_80D	USB	USB_BT_N 14 22
		USB_80D	USB	USB_BT_R_P 22
		USB_80D	USR	USB_BT_R_N 22
	USB_BT	USB_80D	USB	USB_BT_CONN_P
	USB_BT	USB_80D	USB	USB_BT_CONN_N
	USB_TPAD	USB_80D	USR	NC USB_TPADP 14 64
	USB_TPAD	USB_80D	USB	NC USB_TPADN 14 64
	USB_HPM	USB_85D	USR	USB_HPM_P 28 29
	USB_HPM	USB_85D	USR	USB_HPM_N 28 29
		USB_85D	USB	USB_HPM_R_P 26
		USB_85D	USR	USB_HPM_R_N 26
		USB_80D	USB	USB_EXT_A_P 14 26 64
		USB_80D	USR	USB_EXT_A_N 14 26 64
		USB_85D	USR	USB_EXT_A_F_P 26
		USB_85D	USB	USB_EXT_A_F_N
	USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_P 14 29 64
	USB3_EXT_A_RX	USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_N 14 29 64
		USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_C_P
		USB_80D	USB3_PCH_RX	USB3_EXT_A_D2R_C_N
	USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_P 29
	USB3_EXT_A_TX	USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_N 29
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_P 14 29
		USB_80D	USB3_PCH_TX	USB3_EXT_A_R2D_C_N 14 29
		USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_P 14 27
		USB_80D	USB3_PCH_RX	USB3_EXTD_D2R_N 14 27
		USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_P 27 29
		USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_N 27 29
		USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_P 14 29
		USB_80D	USB3_PCH_TX	USB3_EXTD_R2D_C_N 14 29
		UART_45S	UART	SMC_DEBUGPRT_TX_L 26 31 32 64
		UART_45S	UART	SMC_DEBUGPRT_RX_L 26 31 32 64
	USB_EXTB	USB_80D	USB	NC USB_EXTBP 14 64
	USB_EXTB	USB_80D	USB	NC USB_EXTBN 14 64
	USB_EXTB	USB_80D	USB	USB2_EXTB_F_P
	USB_EXTB	USB_80D	USB	USB2_EXTB_F_N
	USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC USB3_EXTB_D2RP 14 64
	USB3_EXTB_RX	USB_80D	USB3_PCH_RX	NC USB3_EXTB_D2RN 14 64
	USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_P
	USB3_EXTB_TX	USB_80D	USB3_PCH_TX	USB3_EXTB_R2D_N
		USB_80D	USB3_PCH_TX	NC USB3_EXTB_R2D_CP 14 64
		USB_80D	USB3_PCH_TX	NC USB3_EXTB_R2D_CN 14 64
	USB_EXTC	USB_80D	USB	USB2_EXTC_P
	USB_EXTC	USB_80D	USB	USB2_EXTC_N
	USB_EXTC	USB_80D	USR	USB2_EXTC_F_P
	USB_EXTC	USB_80D	USB	USB2_EXTC_F_N
	USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_P
	USB3_EXTC_RX	USB_80D	USB3_PCH_RX	USB3_EXTC_D2R_N
	USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_P
	USB3_EXTC_TX	USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_N
		USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_P
		USB_80D	USB3_PCH_TX	USB3_EXTC_R2D_C_N
	USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_P
	USB3_SD_RX	USB_80D	USB3_PCH_RX	USB3RPCIE_SD_D2R_N
	USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_P
	USB3_SD_TX	USB_80D	USB3_PCH_TX	USB3RPCIE_SD_R2D_C_N
		USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_P
		USB_80D	USB3_PCH_RX	USB3_SD_D2R_C_N
		USB_80D	USB3_PCH_TX	USB3_SD_R2D_P
		USB_80D	USB3_PCH_TX	USB3_SD_R2D_N
	PCH_USB_BR1AS	PCH_USB_BR1AS		PCH_USB_BR1AS 14
	PCH_DIFFCCLK_UNUSED	CLK_PCTIE_80D	CLK_PCTIE	PCTIE_CLK100M_PCH_P
	PCH_DIFFCCLK_UNUSED	CLK_PCTIE_80D	CLK_PCTIE	PCTIE_CLK100M_PCH_N
	PCH_DIFFCCLK_UNUSED	CLK_PCTIE_80D	CLK_PCTIE	PCH_CLK96M_DOT_P
	PCH_DIFFCCLK_UNUSED	CLK_PCTIE_80D	CLK_PCTIE	PCH_CLK96M_DOT_N
	PCH_DIFFCCLK_UNUSED	CLK_PCTIE_80D	CLK_PCTIE	PCH_CLK100M_SATA_P
	PCH_DIFFCCLK_UNUSED	CLK_PCTIE_80D	CLK_PCTIE	PCH_CLK100M_SATA_N
		CPU_45S	CLK_PCTIE	PCH_CLK14P3M_REFCLK

Note: 80ohm constraints are actually 85ohm

SYNC MASTER-DEV MLB		SYNC DATE=04/17/2014	
PAGE TITLE			
PCH Constraints 1			
	Apple Inc.	DRAWING NUMBER	SIZE
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	8	7	6	5	4	3	2	1
LPC Bus Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
LPC	*	=3x_DIELECTRIC	?					
CLK_LPC	*	=4x_DIELECTRIC	?					
SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905_v1.5), Section 3.15								
SMBus Interface Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
SMB_45S_R_50S	TOP,BOTTOM	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE			
SMB_45S_R_50S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
SMB	*	=2x_DIELECTRIC	?					
HD Audio Interface Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
HDA	*	=2x_DIELECTRIC	?					
SOURCE: Calpella Platform Design Guide for Ibox Peak M (DG-398905-398905_v1.5), Section 3.15								
SIO Signal Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
CLK_SLOW	*	=4x_DIELECTRIC	?					
SPI Interface Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
SPI	*	=4x_DIELECTRIC	?					
XDP Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
PCH_ITP	*	=2+1_SPACING	?					
DisplayPort								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
DP_2DP	*	=3x_DIELECTRIC	?					
DP_20THERHS	*	=4x_DIELECTRIC	?					
DP_20THER	*	=3x_DIELECTRIC	?					
DP_AUX	*	=3x_DIELECTRIC	?					
NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET					
DP_TX	DP_TX	*	DP_2DP					
DP_TX	*_TX	*	DP_20THERHS					
DP_TX	*_RX	*	DP_20THERHS					
DP_TX	*	*	DP_20THER					
System Clock Signal Constraints								
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP	
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD	
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT					
CLK_SLOW	*	=2x_DIELECTRIC	?					
CLK_25M	*	=5x_DIELECTRIC	?					
NOTE: 25MHz system clocks very sensitive to noise.								

PCH Net Properties					
ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	PHYSICAL	SPACING			
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	14	31
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	14	31
LPC_45S	LPC		LPCPLUS RESET_L		
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC	17	31
	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_SMC_R	12	17
LPC_CLK33M	CLK_LPC_45S	CLK_LPC	LPC_CLK24M_LPCPLUS		
	CLK_LPC_45S	CLK_LPC	TP_LPC_CLK24M_LPCPLUS_R	12	62
SMBUS_PCH_CLK	SMB_45S_R_50S	SMB	SMBUS_PCH_CLK	14	16 34
SMBUS_PCH_DATA	SMB_45S_R_50S	SMB	SMBUS_PCH_DATA	14	16 34
SMBUS_PCH_0_CLK	SMB_45S_R_50S	SMB	SML_PCH_0_CLK	14	34
SMBUS_PCH_0_DATA	SMB_45S_R_50S	SMB	SML_PCH_0_DATA	14	34
SMBUS_SMC_1_S0_SCL	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SCL	14	31 34 36 53 72
SMBUS_SMC_1_S0_SDA	SMB_45S_R_50S	SMB	SMBUS_SMC_1_S0_SDA	14	31 34 36 53 72
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	12	40
HDA_45S	HDA		HDA_BIT_CLK_R	12	
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	12	40
HDA_45S	HDA		HDA_SYNC_R	12	
HDA_RST_L	HDA_45S	HDA	HDA_RST_R_L	12	
HDA_45S	HDA		HDA_RST_L	12	40
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	12	40 64
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	12	40
HDA_45S	HDA		HDA_SDOUT_R	12	17
PM_SUS_CLK	CLK_SLOW_45S	CLK_SLOW	PM_CLK32K_SUSCLK_R	13	32
CLK_SLOW_45S	CLK_SLOW		SMC_CLK32K		
SPT_CLK	SPT_45S	SPT	SPI_CLK_R	14	37
SPT_45S	SPT		SPI_CLK	37	
SPT_MOSI	SPT_45S	SPT	SPI_MOSI_R	14	37
SPT_45S	SPT		SPI_MOSI	37	
SPT_MISO	SPT_45S	SPT	SPI_MISO	14	37
SPT_CS0	SPT_45S	SPT	SPI_CS0_R_L	14	37
SPT_45S	SPT		SPI_CS0_L	37	
SPT_45S	SPT		SPI_SMC_CLK	31	37
SPT_45S	SPT		SPI_SMC_MOSI	31	37
SPT_45S	SPT		SPI_SMC_CS_L	31	37
SPT_45S	SPT		SPI_MLB_CLK	37	
SPT_45S	SPT		SPI_MLB_MOSI	37	
SPT_45S	SPT		SPI_MLB_MISO	37	
SPT_45S	SPT		SPI_MLB_CS_L	37	
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_P	22	
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_N	22	
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	14	22
PCIE_AP_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	14	22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_P	14	22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_N	14	22
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_P	22	
PCIE_AP_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_AP_D2R_C_N	22	
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_P	12	22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_N	12	22
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_P	22	
PCIE_CLK100M_AP	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_AP_C_N	22	
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_P<3..0>		
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_N<3..0>		
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_P<3..0>	14	62
PCIE_TBT_R2D	PCIE_80D	PCIE_PCH_TX	PCIE_TBT_R2D_C_N<3..0>	14	62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_P<3..0>	14	62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_N<3..0>		
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_P<3..0>	14	62
PCIE_TBT_D2R	PCIE_80D	PCIE_PCH_RX	PCIE_TBT_D2R_C_N<3..0>		
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_P	12	29 62 64
PCIE_CLK100M_TBT	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_TBT_N	12	29 62 64
XDP_TDI	PCH_45S	PCH_ITP	XDP_PCH_TDI	12	16
XDP_TDO	PCH_45S	PCH_ITP	XDP_PCH_TDO	12	16
XDP_TMS	PCH_45S	PCH_ITP	XDP_PCH_TMS	12	16
XDP_TCK	PCH_45S	PCH_ITP	XDP_PCH_TCK	12	16
PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_P	24	25
PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_N	24	25
PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_P	14	25
PCIE_CAMERA	PCIE_80D	PCIE_PCH_TX	PCIE_CAMERA_R2D_C_N	14	25
PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_P	14	25 64
PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_N	14	25 64
PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_P	24	25
PCIE_CAMERA	PCIE_80D	PCIE_PCH_RX	PCIE_CAMERA_D2R_C_N	24	25
PCIE_CLK100M_CAMERA	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	12	25
PCIE_CLK100M_CAMERA	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	12	25
PCIE_CLK100M_CAMERA	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	24	25
PCIE_CLK100M_CAMERA	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	24	25
PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_P	24	25
PCIE_CLK100M_DBG	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_DEBUG_N		
DP_TBT_ML	DP_80D	DP_TX	DP_ML_P<3..0>		
DP_TBT_ML	DP_80D	DP_TX	DP_ML_N<3..0>		
DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_P<3..0>		
DP_TBT_ML	DP_80D	DP_TX	DP_ML_C_N<3..0>		
DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_P<3..0>		
DP_TBT_ML	DP_80D	DP_TX	DP_ML_CONN_N<3..0>		
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_P		
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_N		
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_P		
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_C_N		
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_P		
DP_TBT_AUXCH	DP_80D	DP_AUX	DP_AUX_CH_CONN_N		

Clock Net Properties				
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTCX1	
SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK24M_CAMERA	17 24 64
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP_R	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALP	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_XTALN	
	CLK_25M_45S	CLK_25M	CLK25M_CAM_CLKN	24
SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	
SYSCLK_CLK25M_XTAL	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X1	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2	
	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2	5 29
	CLK_25M_45S	CLK_25M	SDCLK_CLK25M_X2_R	
	CLK_25M_45S	CLK_25M	SDSCLK_CLK25M_X1	

E85 Net Properties				
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<0>	5 29
E85_HS_XBAR_D2R	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<0>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<1>	5 29
E85_HS_XBAR_R2D	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<1>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_P<3..2>	5 29
E85_HS	DP_85D	DP_TX	DP_TBTSNK0_ML_C_N<3..2>	5 29
	DP_85D	DP_TX	DP_E85SNK_ML_P<3..0>	27 29
	DP_85D	DP_TX	DP_E85SNK_ML_N<3..0>	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML0_N	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_P	27 29
	DP_85D	DP_TX	E85_HS_DP_ML1_N	27 29
E85_LS	E85_LS_85D	E85_LS	E85_LS_P<2..1>	26 29 64
E85_LS	E85_LS_85D	E85_LS	E85_LS_N<2..1>	26 29 64
	E85_LS_85D	E85_LS	E85_LS_MISSION_P	26
	E85_LS_85D	E85_LS	E85_LS_MISSION_N	26
		E85_CC	E85_CC1	29 60 64
		E85_CC	E85_CC2	29 60 64

Note: 80ohm constraints are actually 85ohm

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_QS2OWNDATA	*	=3x_DIELECTRIC	?
MEM_CMD2CMD	*	=3x_DIELECTRIC	?
MEM_CMD2CTRL	*	=3x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=3x_DIELECTRIC	?
MEM_CLK2CLK	*	=6x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	10000
MEM_2GND	*	=2x_DIELECTRIC	10000
MEM_2OTHER	*	=6x_DIELECTRIC	?

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	MEM_TERM	MEM_70D
MEM_40S	MEM_TERM	MEM_50S

Note: changed MEM_TERM physical rule to MEM_70D from MEM_73D temporarily

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_2OTHER
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_QS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_QS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_QS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_QS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_QS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_QS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_QS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_QS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_QS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_QS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_QS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_QS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_QS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_QS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_QS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	*	*	MEM_2OTHER
MEM_A_DQS_1	*	*	MEM_2OTHER
MEM_A_DQS_2	*	*	MEM_2OTHER
MEM_A_DQS_3	*	*	MEM_2OTHER
MEM_A_DQS_4	*	*	MEM_2OTHER
MEM_A_DQS_5	*	*	MEM_2OTHER
MEM_A_DQS_6	*	*	MEM_2OTHER
MEM_A_DQS_7	*	*	MEM_2OTHER
MEM_B_DQS_0	*	*	MEM_2OTHER
MEM_B_DQS_1	*	*	MEM_2OTHER
MEM_B_DQS_2	*	*	MEM_2OTHER
MEM_B_DQS_3	*	*	MEM_2OTHER
MEM_B_DQS_4	*	*	MEM_2OTHER
MEM_B_DQS_5	*	*	MEM_2OTHER
MEM_B_DQS_6	*	*	MEM_2OTHER
MEM_B_DQS_7	*	*	MEM_2OTHER

MEM_A_DATA_0	*	*	MEM_2OTHER
MEM_A_DATA_1	*	*	MEM_2OTHER
MEM_A_DATA_2	*	*	MEM_2OTHER
MEM_A_DATA_3	*	*	MEM_2OTHER
MEM_A_DATA_4	*	*	MEM_2OTHER
MEM_A_DATA_5	*	*	MEM_2OTHER
MEM_A_DATA_6	*	*	MEM_2OTHER
MEM_A_DATA_7	*	*	MEM_2OTHER
MEM_B_DATA_0	*	*	MEM_2OTHER
MEM_B_DATA_1	*	*	MEM_2OTHER
MEM_B_DATA_2	*	*	MEM_2OTHER
MEM_B_DATA_3	*	*	MEM_2OTHER
MEM_B_DATA_4	*	*	MEM_2OTHER
MEM_B_DATA_5	*	*	MEM_2OTHER
MEM_B_DATA_6	*	*	MEM_2OTHER
MEM_B_DATA_7	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_A_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_0	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_1	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_2	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_3	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_4	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_5	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_6	MEM_*_DATA_*	*	MEM_2OTHERMEM
MEM_B_DATA_7	MEM_*_DATA_*	*	MEM_2OTHERMEM

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET TYPE		
	PHYSICAL	SPACING	
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_P<0>
MEM_A_CLK0	MEM_70D	MEM_CLK	MEM_A_CLK_N<0>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_P<1>
MEM_A_CLK1	MEM_70D	MEM_CLK	MEM_A_CLK_N<1>
MEM_A_CS0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0>
MEM_A_CS1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1>
MEM_A_ODT	MEM_40S	MEM_CTRL	MEM_A_ODT<0>
MEM_A_CKE0	MEM_40S	MEM_CMD	MEM_A_CKE<1..0>
MEM_A_CKE1	MEM_40S	MEM_CMD	MEM_A_CKE<3..2>
MEM_A_CMD0	MEM_40S	MEM_CMD	MEM_A_CAA<9..0>
MEM_A_CMD1	MEM_40S	MEM_CMD	MEM_A_CAB<9..0>
MEM_A_DO_BYTE0	MEM_40S	MEM_A_DATA_0	MEM_A_DO<7..0>
MEM_A_DO_BYTE1	MEM_40S	MEM_A_DATA_1	MEM_A_DO<15..8>
MEM_A_DO_BYTE2	MEM_40S	MEM_A_DATA_2	MEM_A_DO<23..16>
MEM_A_DO_BYTE3	MEM_40S	MEM_A_DATA_3	MEM_A_DO<31..24>
MEM_A_DO_BYTE4	MEM_40S	MEM_A_DATA_4	MEM_A_DO<39..32>
MEM_A_DO_BYTE5	MEM_40S	MEM_A_DATA_5	MEM_A_DO<47..40>
MEM_A_DO_BYTE6	MEM_40S	MEM_A_DATA_6	MEM_A_DO<55..48>
MEM_A_DO_BYTE7	MEM_40S	MEM_A_DATA_7	MEM_A_DO<63..56>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_P<0>
MEM_A_DQS0	MEM_70D	MEM_A_DQS_0	MEM_A_DQS_N<0>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_P<1>
MEM_A_DQS1	MEM_70D	MEM_A_DQS_1	MEM_A_DQS_N<1>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_P<2>
MEM_A_DQS2	MEM_70D	MEM_A_DQS_2	MEM_A_DQS_N<2>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_P<3>
MEM_A_DQS3	MEM_70D	MEM_A_DQS_3	MEM_A_DQS_N<3>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_P<4>
MEM_A_DQS4	MEM_70D	MEM_A_DQS_4	MEM_A_DQS_N<4>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_P<5>
MEM_A_DQS5	MEM_70D	MEM_A_DQS_5	MEM_A_DQS_N<5>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_P<6>
MEM_A_DQS6	MEM_70D	MEM_A_DQS_6	MEM_A_DQS_N<6>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_P<7>
MEM_A_DQS7	MEM_70D	MEM_A_DQS_7	MEM_A_DQS_N<7>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_P<0>
MEM_B_CLK0	MEM_70D	MEM_CLK	MEM_B_CLK_N<0>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_P<1>
MEM_B_CLK1	MEM_70D	MEM_CLK	MEM_B_CLK_N<1>
MEM_B_CS0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0>
MEM_B_CS1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1>
MEM_B_ODT	MEM_40S	MEM_CTRL	MEM_B_ODT<0>
MEM_B_CKE0	MEM_40S	MEM_CMD	MEM_B_CKE<1..0>
MEM_B_CKE1	MEM_40S	MEM_CMD	MEM_B_CKE<3..2>
MEM_B_CMD0	MEM_40S	MEM_CMD	MEM_B_CAA<9..0>
MEM_B_CMD1	MEM_40S	MEM_CMD	MEM_B_CAB<9..0>
MEM_B_DO_BYTE0	MEM_40S	MEM_B_DATA_0	MEM_B_DO<7..0>
MEM_B_DO_BYTE1	MEM_40S	MEM_B_DATA_1	MEM_B_DO<15..8>
MEM_B_DO_BYTE2	MEM_40S	MEM_B_DATA_2	MEM_B_DO<23..16>
MEM_B_DO_BYTE3	MEM_40S	MEM_B_DATA_3	MEM_B_DO<31..24>
MEM_B_DO_BYTE4	MEM_40S	MEM_B_DATA_4	MEM_B_DO<39..32>
MEM_B_DO_BYTE5	MEM_40S	MEM_B_DATA_5	MEM_B_DO<47..40>
MEM_B_DO_BYTE6	MEM_40S	MEM_B_DATA_6	MEM_B_DO<55..48>
MEM_B_DO_BYTE7	MEM_40S	MEM_B_DATA_7	MEM_B_DO<63..56>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_P<0>
MEM_B_DQS0	MEM_70D	MEM_B_DQS_0	MEM_B_DQS_N<0>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_P<1>
MEM_B_DQS1	MEM_70D	MEM_B_DQS_1	MEM_B_DQS_N<1>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_P<2>
MEM_B_DQS2	MEM_70D	MEM_B_DQS_2	MEM_B_DQS_N<2>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_P<3>
MEM_B_DQS3	MEM_70D	MEM_B_DQS_3	MEM_B_DQS_N<3>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_P<4>
MEM_B_DQS4	MEM_70D	MEM_B_DQS_4	MEM_B_DQS_N<4>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_P<5>
MEM_B_DQS5	MEM_70D	MEM_B_DQS_5	MEM_B_DQS_N<5>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_P<6>
MEM_B_DQS6	MEM_70D	MEM_B_DQS_6	MEM_B_DQS_N<6>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_P<7>
MEM_B_DQS7	MEM_70D	MEM_B_DQS_7	MEM_B_DQS_N<7>
		MEM_PWR	PP1V2_S3
		MEM_PWR	PPVREF_S3 MEM_VREFCA
		MEM_PWR	PPVREF_S3 MEM_VREFDO_A
		MEM_PWR	PPVREF_S3 MEM_VREFCA
		MEM_PWR	PPVREF_S3 MEM_VREFDO_B

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PAGE TITLE

Memory Constraints

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NAND BUS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
NAND_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
NAND_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
NAND_QOS	*	0.100 MM	?
NAND_IO	*	0.100 MM	?
NAND_CMD	*	0.100 MM	?

NAND :

DQS_P/N MAX LENGTH 3"
IO<7..0> SIGNALS SHOULD MATCH +/- 50MIL FROM DQS_P/N
IO<7..0> AND ASSOCIATED DQS_P/N ROUTE ON SAME LAYER. NO MORE THAN 2 VIA TRANSITIONS.
NCE<7..0>,ALE,CLE SHOULD MATCH +/- 250MIL FROM NWE
DQS_P/N & NRE_P/N SHOULD MATCH +/- 100MIL FROM NWE

NAND NET PROPERTIES

ELECTRICAL CONSTRAINT_SET	NET TYPE			
	PHYSICAL	SPACING		
H240 ANI0_IO	NAND_45S	NAND_TO	ANI0_IO<7..0>	55 58
H240 DP_ANI0_DOS	NAND_85D	NAND_DOS	ANI0_DOS_P	55 58
H240 DP_ANI0_DOS	NAND_85D	NAND_DOS	ANI0_DOS_N	55 58
H240 DP_ANI0_NRE	NAND_85D	NAND_DOS	ANI0_NRE_P	55 58
H240 DP_ANI0_NRE	NAND_85D	NAND_DOS	ANI0_NRE_N	55 58
H240 ANI0_NWE	NAND_45S	NAND_CMD	ANI0_NWE	55 58
H240 ANI0_NCE	NAND_45S	NAND_CMD	ANI0_NCE<3..0>	55 58
H240 ANI0_ALE	NAND_45S	NAND_CMD	ANI0_ALE	55 58
H240 ANI0_CLE	NAND_45S	NAND_CMD	ANI0_CLE	55 58
H240 ANI1_IO	NAND_45S	NAND_TO	ANI1_IO<7..0>	55 58
H240 DP_ANI1_DOS	NAND_85D	NAND_DOS	ANI1_DOS_P	55 58
H240 DP_ANI1_DOS	NAND_85D	NAND_DOS	ANI1_DOS_N	55 58
H240 DP_ANI1_NRE	NAND_85D	NAND_DOS	ANI1_NRE_P	55 58
H240 DP_ANI1_NRE	NAND_85D	NAND_DOS	ANI1_NRE_N	55 58
H240 ANI1_NWE	NAND_45S	NAND_CMD	ANI1_NWE	55 58
H240 ANI1_NCE	NAND_45S	NAND_CMD	ANI1_NCE<3..0>	55 58
H240 ANI1_ALE	NAND_45S	NAND_CMD	ANI1_ALE	55 58
H240 ANI1_CLE	NAND_45S	NAND_CMD	ANI1_CLE	55 58
H240 ANI2_IO	NAND_45S	NAND_TO	ANI2_IO<7..0>	
H240 DP_ANI2_DOS	NAND_85D	NAND_DOS	ANI2_DOS_P	
H240 DP_ANI2_DOS	NAND_85D	NAND_DOS	ANI2_DOS_N	
H240 DP_ANI2_NRE	NAND_85D	NAND_DOS	ANI2_NRE_P	
H240 DP_ANI2_NRE	NAND_85D	NAND_DOS	ANI2_NRE_N	
H240 ANI2_NWE	NAND_45S	NAND_CMD	ANI2_NWE	
H240 ANI2_NCE	NAND_45S	NAND_CMD	ANI2_NCE<3..0>	
H240 ANI2_ALE	NAND_45S	NAND_CMD	ANI2_ALE	
H240 ANI2_CLE	NAND_45S	NAND_CMD	ANI2_CLE	
H240 ANI3_IO	NAND_45S	NAND_TO	ANI3_IO<7..0>	
H240 DP_ANI3_DOS	NAND_85D	NAND_DOS	ANI3_DOS_P	
H240 DP_ANI3_DOS	NAND_85D	NAND_DOS	ANI3_DOS_N	
H240 DP_ANI3_NRE	NAND_85D	NAND_DOS	ANI3_NRE_P	
H240 DP_ANI3_NRE	NAND_85D	NAND_DOS	ANI3_NRE_N	
H240 ANI3_NWE	NAND_45S	NAND_CMD	ANI3_NWE	
H240 ANI3_NCE	NAND_45S	NAND_CMD	ANI3_NCE<3..0>	
H240 ANI3_ALE	NAND_45S	NAND_CMD	ANI3_ALE	
H240 ANI3_CLE	NAND_45S	NAND_CMD	ANI3_CLE	

NAND NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
AN14_IO		NAND_45S	NAND_TO	AN14_IO<7..0>
DP_AN14_DOS		NAND_85D	NAND_DOS	AN14_DOS_P
DP_AN14_DOS		NAND_85D	NAND_DOS	AN14_DOS_N
DP_AN14_NRE		NAND_85D	NAND_DOS	AN14_NRE_P
DP_AN14_NRE		NAND_85D	NAND_DOS	AN14_NRE_N
AN14_NWE		NAND_45S	NAND_CMD	AN14_NWE
AN14_NCE		NAND_45S	NAND_CMD	AN14_NCE<3..0>
AN14_ALE		NAND_45S	NAND_CMD	AN14_ALE
AN14_CLE		NAND_45S	NAND_CMD	AN14_CLE
AN15_IO		NAND_45S	NAND_TO	AN15_IO<7..0>
DP_AN15_DOS		NAND_85D	NAND_DOS	AN15_DOS_P
DP_AN15_DOS		NAND_85D	NAND_DOS	AN15_DOS_N
DP_AN15_NRE		NAND_85D	NAND_DOS	AN15_NRE_P
DP_AN15_NRE		NAND_85D	NAND_DOS	AN15_NRE_N
AN15_NWE		NAND_45S	NAND_CMD	AN15_NWE
AN15_NCE		NAND_45S	NAND_CMD	AN15_NCE<3..0>
AN15_ALE		NAND_45S	NAND_CMD	AN15_ALE
AN15_CLE		NAND_45S	NAND_CMD	AN15_CLE
AN16_IO		NAND_45S	NAND_TO	AN16_IO<7..0>
DP_AN16_DOS		NAND_85D	NAND_DOS	AN16_DOS_P
DP_AN16_DOS		NAND_85D	NAND_DOS	AN16_DOS_N
DP_AN16_NRE		NAND_85D	NAND_DOS	AN16_NRE_P
DP_AN16_NRE		NAND_85D	NAND_DOS	AN16_NRE_N
AN16_NWE		NAND_45S	NAND_CMD	AN16_NWE
AN16_NCE		NAND_45S	NAND_CMD	AN16_NCE<3..0>
AN16_ALE		NAND_45S	NAND_CMD	AN16_ALE
AN16_CLE		NAND_45S	NAND_CMD	AN16_CLE
AN17_IO		NAND_45S	NAND_TO	AN17_IO<7..0>
DP_AN17_DOS		NAND_85D	NAND_DOS	AN17_DOS_P
DP_AN17_DOS		NAND_85D	NAND_DOS	AN17_DOS_N
DP_AN17_NRE		NAND_85D	NAND_DOS	AN17_NRE_P
DP_AN17_NRE		NAND_85D	NAND_DOS	AN17_NRE_N
AN17_NWE		NAND_45S	NAND_CMD	AN17_NWE
AN17_NCE		NAND_45S	NAND_CMD	AN17_NCE<3..0>
AN17_ALE		NAND_45S	NAND_CMD	AN17_ALE
AN17_CLE		NAND_45S	NAND_CMD	AN17_CLE

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT


Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
S2_MEM_CLK	S2_MFM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 24 25
S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 24 25
S2_MEM_CNTL	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_CKE 24 25
S2_MEM_CNTL	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 24 25 64
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_ODT 25
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 24 25
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 24 25
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_WE_L 24 25
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 24 25
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 24 25
S2_MEM_CMD	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 24 25
S2_MEM_DQS0	S2_MFM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 24 25
S2_MEM_DQS0	S2_MFM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 24 25
S2_MEM_DQS1	S2_MFM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 24 25
S2_MEM_DQS1	S2_MFM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 24 25
S2_MEM_DATA_0	S2_MFM_45S	S2_MFM_DATA0	MEM_CAM_DM<0> 24 25
S2_MEM_DATA_1	S2_MFM_45S	S2_MFM_DATA1	MEM_CAM_DM<1> 24 25
S2_MEM_A	S2_MFM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 24 25 64
S2_MEM_DATA_0	S2_MFM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 24 25
S2_MEM_DATA_1	S2_MFM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 24 25
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 24 25
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 24 25
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 25 53
MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 25 53
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 24 25
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 24 25
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 25 53
MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 25 53
		S2_MEM_PWR	PP1V35_CAM 24 25
		S2_MEM_PWR	PP0V675_CAM_VREF 24 25
		S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 25

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Camera Constraints			
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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SENSE_1T01_P2MM	*	=1T01_DIFFPAIR	0.200 MM	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SENSE_1T01_P3MM	*	=1T01_DIFFPAIR	0.300 MM	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR
THERM_1T01_45S	*	=1T01_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1T01_DIFFPAIR	=1T01_DIFFPAIR
SPKR_DIFFPAIR	*	=1T01_DIFFPAIR	0.400 MM	0.100 MM	=1T01_DIFFPAIR	=1T01_DIFFPAIR	=1T01_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=1:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
GND	LVDS*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	10000
PWR_P2MM	*	0.20 MM	10000

RF Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
RF_50S	*	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=50_OHM_SE_RF	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
RF	*	0.15 MM	?

J92 MLB Specific Net Properties

ELECTRICAL_CONSTRAINT_SET		PHYSICAL	NET_TYPE	SPACING	
					ISNS_HS_GAIN_P
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			ISNS_HS_GAIN_P
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			ISNS_HS_GAIN_N
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			ISNS_HS_COMPUTING_N
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			ISNS_HS_COMPUTING_P
SENSE_DIFFPAIR	THERM_I101_45S	THERM			INLET_THMSNS_D1_P
SENSE_DIFFPAIR	THERM_I101_45S	THERM			INLET_THMSNS_D1_N
SENSE_DIFFPAIR	SENSE_I101_P3MM	SENSE			ISNS_I1V2_S3_P
SENSE_DIFFPAIR	SENSE_I101_P3MM	SENSE			ISNS_I1V2_S3_N
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			ISNS_ICDBKLT_P
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			ISNS_ICDBKLT_N
SENSE_DIFFPAIR	SENSE_I101_P2MM	SENSE			ISNS_I1V05_SUS_P
SENSE_DIFFPAIR	SENSE_I101_P2MM	SENSE			ISNS_I1V05_SUS_N
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			CPUVR_ISNS1_P
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			CPUVR_ISNS1_N
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			CPUVR_ISNS2_P
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			CPUVR_ISNS2_N
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			CPUTHMSNS_D2_P
SENSE_DIFFPAIR	SENSE_I101_45S	SENSE			CPUTHMSNS_D2_N
	I101_DIFFPAIR	AUDIO			MAX98300_R_P
	I101_DIFFPAIR	AUDIO			MAX98300_R_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_ROUTE1_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_ROUTE1_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_ROUTE2_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_ROUTE2_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_LOUT1_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_LOUT1_N
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_LOUT2_P
SPKR_OUT	SPKR_DIFFPAIR	AUDIO			SPKRAMP_LOUT2_N
		SR_POWER			PP3V3_S5
		SR_POWER			PP3V3_S0
		GND			GND
	RF_50S	RF			RF_A_0_DIPLEXER
	RF_50S	RF			RF_A_0_MATCH
	RF_50S	RF			RF_G_0_DIPLEXER
	RF_50S	RF			RF_G_0_MATCH
	RF_50S	RF			RF_0_ANT
	RF_50S	RF			RF_0_ANT_MATCH_T
	RF_50S	RF			RF_A_1_DIPLEXER
	RF_50S	RF			RF_A_1_MATCH
	RF_50S	RF			RF_G_1_DIPLEXER
	RF_50S	RF			RF_G_1_MATCH
	RF_50S	RF			RF_1_ANT
	RF_50S	RF			RF_1_ANT_MATCH_T
DP_EXT_ML	DP_80D	DP_TX			DP_EXT_ML_P<1..0>
DP_EXT_ML	DP_80D	DP_TX			DP_EXT_ML_N<1..0>
	DP_80D	DP_TX			DP_EXT_ML_C_P<1..0>
	DP_80D	DP_TX			DP_EXT_ML_C_N<1..0>
USB_EXT_A	USB_80D	USB			DPRUSB_EXT_A_P
USB_EXT_A	USB_80D	USB			DPRUSB_EXT_A_N
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX			DPRUSB3_EXT_A_D2R_P
USB3_EXT_A_RX	USB_80D	USB3_PCH_RX			DPRUSB3_EXT_A_D2R_N
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX			DPRUSB3_EXT_A_R2D_P
USB3_EXT_A_TX	USB_80D	USB3_PCH_TX			DPRUSB3_EXT_A_R2D_N

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